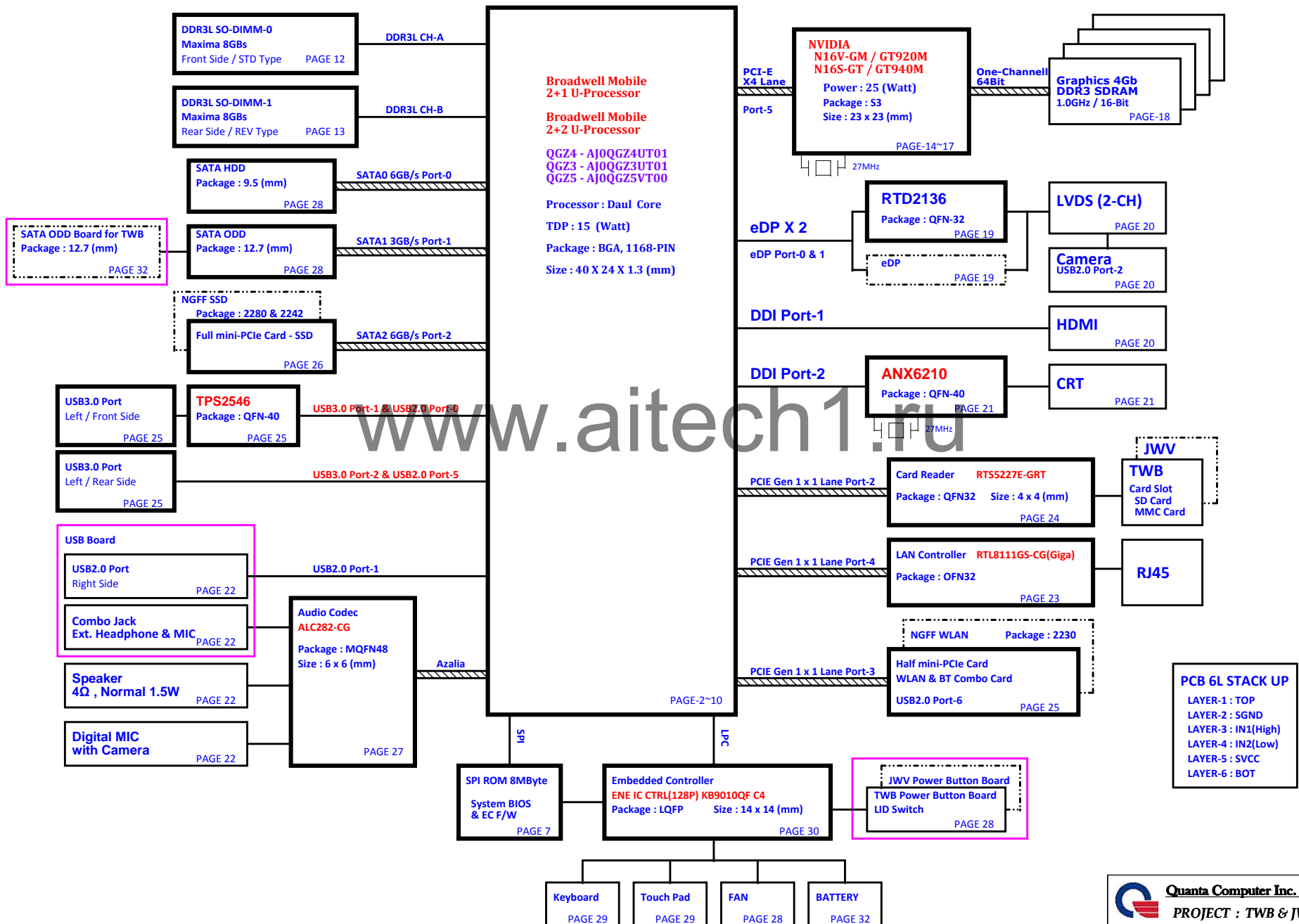
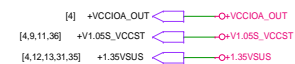
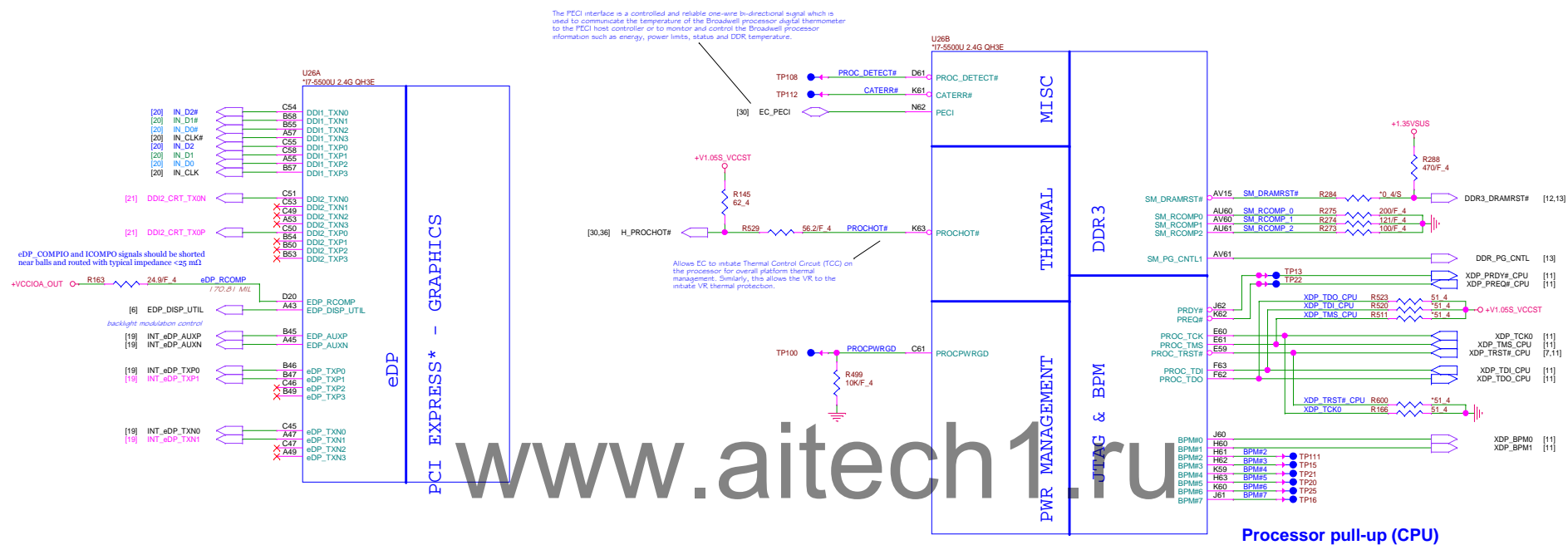


TWB + JWV Intel Boardwell ULT Platform Block Diagram





Haswell ULT Processor (DDR3L)

[12] M_A_DQ[0:3]
[13] M_B_DQ[0:3]
[12] M_A_DQSN[7:0]
[12] M_A_DQSP[7:0]
[13] M_B_DQSN[7:0]
[13] M_B_DQSP[7:0]

U26C
17-5500U 2.4G QH3E

M_A_DQ0 AH83 SA_DQ0
M_A_DQ1 AH82 SA_DQ1
M_A_DQ2 AH83 SA_DQ2
M_A_DQ3 AH81 SA_DQ3
M_A_DQ4 AH81 SA_DQ4
M_A_DQ5 AH80 SA_DQ5
M_A_DQ6 AK61 SA_DQ6
M_A_DQ7 AK60 SA_DQ7
M_A_DQ8 AM63 SA_DQ8
M_A_DQ9 AM62 SA_DQ9
M_A_DQ10 AP63 SA_DQ10
M_A_DQ11 AP62 SA_DQ11
M_A_DQ12 AM61 SA_DQ12
M_A_DQ13 AM60 SA_DQ13
M_A_DQ14 AP61 SA_DQ14
M_A_DQ15 AP60 SA_DQ15
M_B_DQ0 AP58 SA_DQ16
M_B_DQ1 AR58 SA_DQ17
M_B_DQ2 AM67 SA_DQ18
M_B_DQ3 AK57 SA_DQ19
M_B_DQ4 AL56 SA_DQ20
M_B_DQ5 AK58 SA_DQ21
M_B_DQ6 AR57 SA_DQ22
M_B_DQ7 AR57 SA_DQ23
M_B_DQ8 AP55 SA_DQ24
M_B_DQ9 AR55 SA_DQ25
M_B_DQ10 AK54 SA_DQ26
M_B_DQ11 AK54 SA_DQ27
M_B_DQ12 AL55 SA_DQ28
M_B_DQ13 AK55 SA_DQ29
M_B_DQ14 AR54 SA_DQ30
M_B_DQ15 AR54 SA_DQ31
M_A_DQ16 AY58 SA_DQ32
M_A_DQ17 AW58 SA_DQ33
M_A_DQ18 AY56 SA_DQ34
M_A_DQ19 AW56 SA_DQ35
M_A_DQ20 AU58 SA_DQ36
M_A_DQ21 AU58 SA_DQ37
M_A_DQ22 AU56 SA_DQ38
M_A_DQ23 AU54 SA_DQ39
M_A_DQ24 AW54 SA_DQ40
M_A_DQ25 AY52 SA_DQ41
M_A_DQ26 AW52 SA_DQ42
M_A_DQ27 AW52 SA_DQ43
M_A_DQ28 AV54 SA_DQ44
M_A_DQ29 AU54 SA_DQ45
M_A_DQ30 AV52 SA_DQ46
M_A_DQ31 AU52 SA_DQ47
M_B_DQ32 AK40 SA_DQ48
M_B_DQ33 AK42 SA_DQ49
M_B_DQ34 AM43 SA_DQ50
M_B_DQ35 AM45 SA_DQ51
M_B_DQ36 AK45 SA_DQ52
M_B_DQ37 AK43 SA_DQ53
M_B_DQ38 AK40 SA_DQ54
M_B_DQ39 AM42 SA_DQ55
M_B_DQ40 AM46 SA_DQ56
M_B_DQ41 AK46 SA_DQ57
M_B_DQ42 AM49 SA_DQ58
M_B_DQ43 AK49 SA_DQ59
M_B_DQ44 AM48 SA_DQ60
M_B_DQ45 AK48 SA_DQ61
M_B_DQ46 AM51 SA_DQ62
M_B_DQ47 AK51 SA_DQ63

DDR SYSTEM MEMORY A

SA_CLK0 AV37 M_A_CLKP0 [12]
SA_CLK#0 AU37 M_A_CLKN0 [12]
SA_CKE0 AU43 M_A_CKE0 [12]

SA_CLK1 AY36 M_A_CLKP1 [12]
SA_CLK#1 AW36 M_A_CLKN1 [12]
SA_CKE1 AW43 M_A_CKE1 [12]

SA_CKE2 AY42

SA_CKE3 AY43

SA_CS#0 AP33 M_A_CS#0 [12]
SA_CS#1 AR32 M_A_CS#1 [12]

SA_ODT0 AP32 TP66

SA_DQSN0 AJ61 M_A_DQSN0
SA_DQSN1 AM62 M_A_DQSN1
SA_DQSN2 AM58 M_B_DQSN0
SA_DQSN3 AM55 M_B_DQSN1
SA_DQSN4 AV57 M_A_DQSN2
SA_DQSN5 AY63 M_A_DQSN3
SA_DQSN6 AL43 M_B_DQSN2
SA_DQSN7 AL48 M_B_DQSN3

SA_DQSP0 AJ62 M_A_DQSP0
SA_DQSP1 AN61 M_A_DQSP1
SA_DQSP2 AN58 M_B_DQSP0
SA_DQSP3 AN55 M_B_DQSP1
SA_DQSP4 AW57 M_A_DQSP2
SA_DQSP5 AW53 M_A_DQSP3
SA_DQSP6 AL42 M_B_DQSP2
SA_DQSP7 AL49 M_B_DQSP3

SA_MA0 AU36 M_A_A0
SA_MA1 AY37 M_A_A1
SA_MA2 AR38 M_A_A2
SA_MA3 AP36 M_A_A3
SA_MA4 AU39 M_A_A4
SA_MA5 AR36 M_A_A5
SA_MA6 AV40 M_A_A6
SA_MA7 AW39 M_A_A7
SA_MA8 AY38 M_A_A8
SA_MA9 AP35 M_A_A9
SA_MA10 AW41 M_A_A10
SA_MA11 AU41 M_A_A11
SA_MA12 AR35 M_A_A12
SA_MA13 AV42 M_A_A13
SA_MA14 AU42 M_A_A14
SA_MA15

SM_VREF_CA SM_VREF_DQ0 SM_VREF_DQ1
AP49 SMDDR_VREF_DQ0_M3 [12]
AR51 SMDDR_VREF_DQ1_M3 [13]
AP51

VIA: VIA2001/OA25 check match 20milP
VREF_CA : Command / Address Reference Voltage.
VREF_DQ_A, VREF_DQ_B : Data Reference Voltage.

20mils width

U26D
17-5500U 2.4G QH3E

M_B_DQ32 AY31 SB_DQ0
M_B_DQ33 AW31 SB_DQ1
M_B_DQ34 AY29 SB_DQ2
M_B_DQ35 AW29 SB_DQ3
M_B_DQ36 AV31 SB_DQ4
M_B_DQ37 AU31 SB_DQ5
M_B_DQ38 AY29 SB_DQ6
M_B_DQ39 AU29 SB_DQ7
M_B_DQ40 AY27 SB_DQ8
M_B_DQ41 AW27 SB_DQ9
M_B_DQ42 AY25 SB_DQ10
M_B_DQ43 AW25 SB_DQ11
M_B_DQ44 AU27 SB_DQ12
M_B_DQ45 AU27 SB_DQ13
M_B_DQ46 AY25 SB_DQ14
M_B_DQ47 AU25 SB_DQ15
M_B_DQ48 AM29 SB_DQ16
M_B_DQ49 AK29 SB_DQ17
M_B_DQ50 AL28 SB_DQ18
M_B_DQ51 AK28 SB_DQ19
M_B_DQ52 AN29 SB_DQ20
M_B_DQ53 AR28 SB_DQ21
M_B_DQ54 AP28 SB_DQ22
M_B_DQ55 AN26 SB_DQ23
M_B_DQ56 AR26 SB_DQ24
M_B_DQ57 AR26 SB_DQ25
M_B_DQ58 AP25 SB_DQ26
M_B_DQ59 AK26 SB_DQ27
M_B_DQ60 AK26 SB_DQ28
M_B_DQ61 AK26 SB_DQ29
M_B_DQ62 AL26 SB_DQ30
M_B_DQ63 AY23 SB_DQ31
M_B_DQ64 AW23 SB_DQ32
M_B_DQ65 AY21 SB_DQ33
M_B_DQ66 AV21 SB_DQ34
M_B_DQ67 AU23 SB_DQ35
M_B_DQ68 AU23 SB_DQ36
M_B_DQ69 AV21 SB_DQ37
M_B_DQ70 AU21 SB_DQ38
M_B_DQ71 AU21 SB_DQ39
M_B_DQ72 AW19 SB_DQ40
M_B_DQ73 AW17 SB_DQ41
M_B_DQ74 AW17 SB_DQ42
M_B_DQ75 AV19 SB_DQ43
M_B_DQ76 AV19 SB_DQ44
M_B_DQ77 AU19 SB_DQ45
M_B_DQ78 AY17 SB_DQ46
M_B_DQ79 AY17 SB_DQ47
M_B_DQ80 AR21 SB_DQ48
M_B_DQ81 AR22 SB_DQ49
M_B_DQ82 AL21 SB_DQ50
M_B_DQ83 AM22 SB_DQ51
M_B_DQ84 AP22 SB_DQ52
M_B_DQ85 AK21 SB_DQ53
M_B_DQ86 AK22 SB_DQ54
M_B_DQ87 AN20 SB_DQ55
M_B_DQ88 AR20 SB_DQ56
M_B_DQ89 AK18 SB_DQ57
M_B_DQ90 AL18 SB_DQ58
M_B_DQ91 AK20 SB_DQ59
M_B_DQ92 AM20 SB_DQ60
M_B_DQ93 AR18 SB_DQ61
M_B_DQ94 AP18 SB_DQ62
M_B_DQ95 AP18 SB_DQ63

DDR SYSTEM MEMORY B

SB_CLK0 AN38 M_B_CLKP0 [13]
SB_CLK#0 AM38 M_B_CLKN0 [13]
SB_CKE0 AY49 M_B_CKE0 [13]

SB_CLK1 AL38 M_B_CLKP1 [13]
SB_CLK#1 AK38 M_B_CLKN1 [13]
SB_CKE1 AU50 M_B_CKE1 [13]

SB_CKE2 AW48

SB_CKE3 AV50

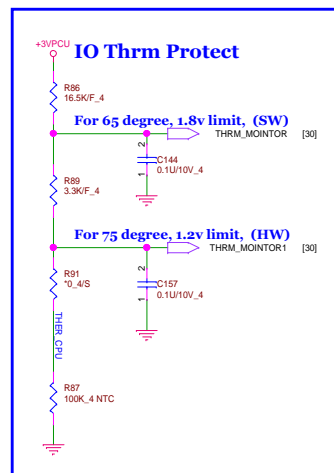
SB_CS#0 AM52 M_B_CS#0 [13]
SB_CS#1 AK32 M_B_CS#1 [13]

SB_ODT0 AL32 TP54

SB_DQSN0 AW30 M_A_DQSN4
SB_DQSN1 AV28 M_A_DQSN5
SB_DQSN2 AN28 M_B_DQSN4
SB_DQSN3 AN25 M_B_DQSN5
SB_DQSN4 AW22 M_A_DQSN6
SB_DQSN5 AV18 M_A_DQSN7
SB_DQSN6 AN21 M_B_DQSN6
SB_DQSN7 AN18 M_B_DQSN7

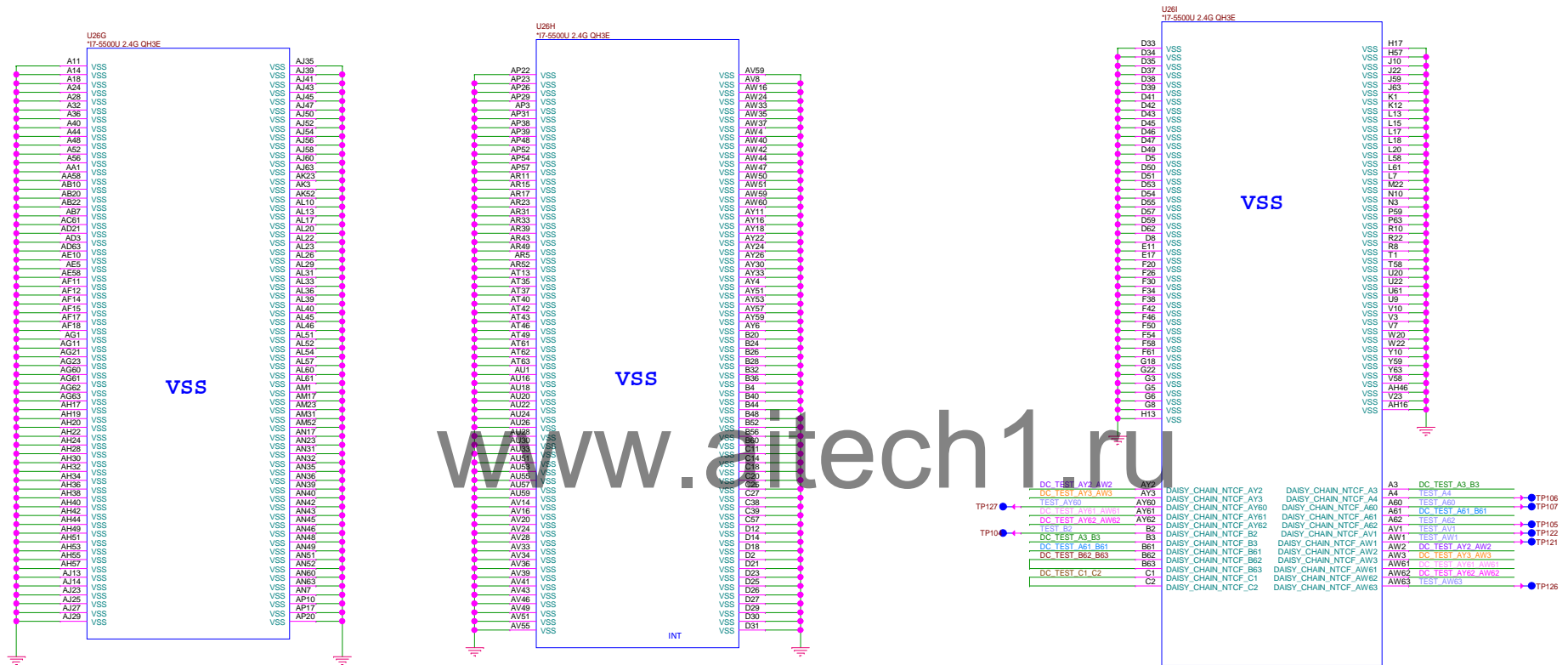
SB_DQSP0 AW30 M_A_DQSP4
SB_DQSP1 AW26 M_A_DQSP5
SB_DQSP2 AM25 M_B_DQSP4
SB_DQSP3 AV22 M_A_DQSP5
SB_DQSP4 AW18 M_A_DQSP6
SB_DQSP5 AM21 M_B_DQSP6
SB_DQSP6 AM18 M_B_DQSP7
SB_DQSP7

SB_MA0 AP40 M_B_A0
SB_MA1 AR40 M_B_A1
SB_MA2 AP42 M_B_A2
SB_MA3 AR42 M_B_A3
SB_MA4 AR45 M_B_A4
SB_MA5 AP45 M_B_A5
SB_MA6 AY46 M_B_A6
SB_MA7 AY47 M_B_A7
SB_MA8 AU46 M_B_A8
SB_MA9 AK36 M_B_A9
SB_MA10 AW47 M_B_A10
SB_MA11 AU47 M_B_A11
SB_MA12 AK33 M_B_A12
SB_MA13 AR46 M_B_A13
SB_MA14 AP46 M_B_A14
SB_MA15



- * The CFG signals have a default value of "1" if not terminated on the board.
- * CFG[3] : MSR Privacy Bit Feature,
 - ("1" = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting.
 - * "0" = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden.)
- * CFG[4] : eDP enable, ("1" = Disabled, "0" = Enabled)

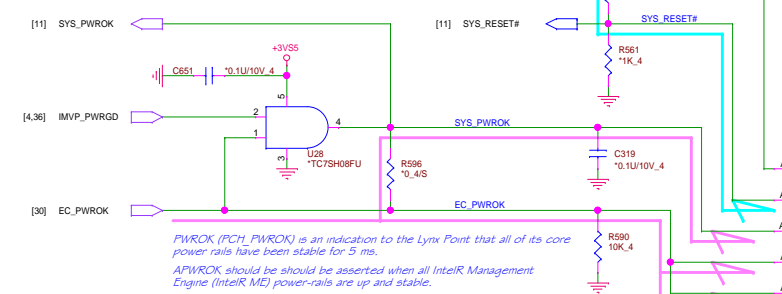
Figure 1: Pin configuration for the PicoBlaze module. The diagram shows a 40-pin connector with pins numbered 1 to 40. Pins 2, 3, 36, and 6 are labeled with their functions: +VCCIOA_OUT, +3VPCU, +VCC_CORE, and +VCCIO_OUT respectively. Pins 2, 3, 36, and 6 are also labeled with their corresponding pin numbers in brackets: [2], [3], [36], and [6]. Pins 2, 3, 36, and 6 are connected to the module's internal circuitry. Pins 2, 3, 36, and 6 are also labeled with their corresponding pin numbers in brackets: [2], [3], [36], and [6]. Pins 2, 3, 36, and 6 are connected to the module's internal circuitry.



Lynx Point-LP Platform Controller Hub (LVDS,DDI)

System PWR_OK(CLG)
SYS_PWROK is used to inform the Lynx Point that power is stable to some other system component(s) and the system is ready to start the exit from reset.

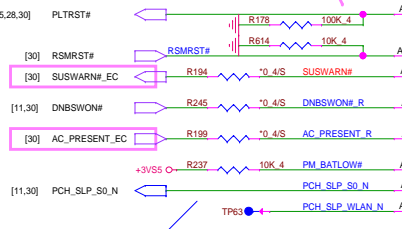
SYS_RESET#
Input to PCH M cannot float. This pin forces an internal reset to the PCH.



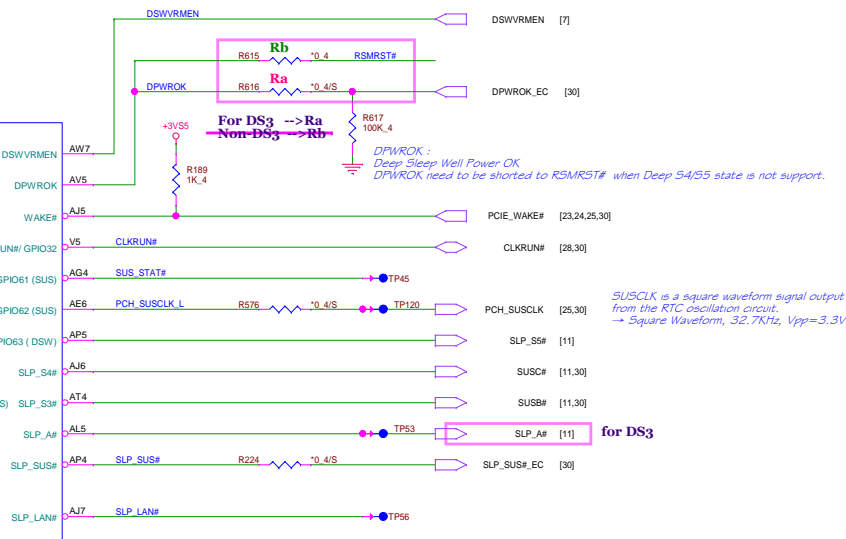
PWROK (PCH_PWROK) is an indication to the Lynx Point that all of its core power rails have been stable for 5 ms.
APWROK should be asserted when all Intel® Management Engine (Intel® ME) power-rails are up and stable.

SUSPWRDNACK / SUSWARN#
This signal is Active-high and is driven low by the Intel® ME when it requires the PCH Suspend Well to be powered.

for DS3



SLP_S0# is a PCH signal which indicates the system is in the S0 state. SLP_S0# stays high in Sx and during S0 exit. This signal will be low during low power states.



For DS3 --> Ra
Non-DS3 --> Rb

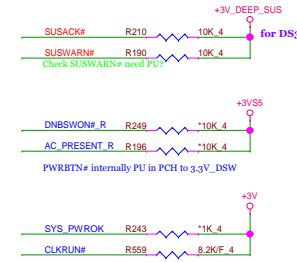
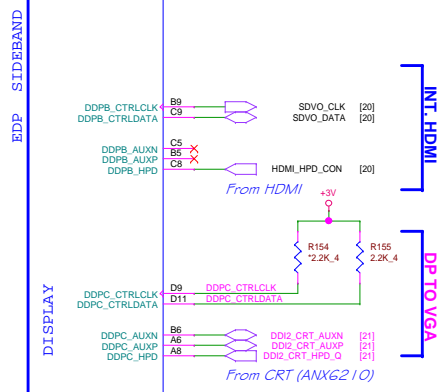
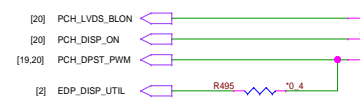
DPWROK : Deep Sleep Well Power OK.
DPWROK need to be shorted to RSMRST# when Deep S4/S5 state is not support.

SUSCLK is a square waveform signal output from the RTC oscillation circuit.
→ Square Waveform, 32.7KHz, Vpp=3.3V.

for DS3

www.aitech1.ru

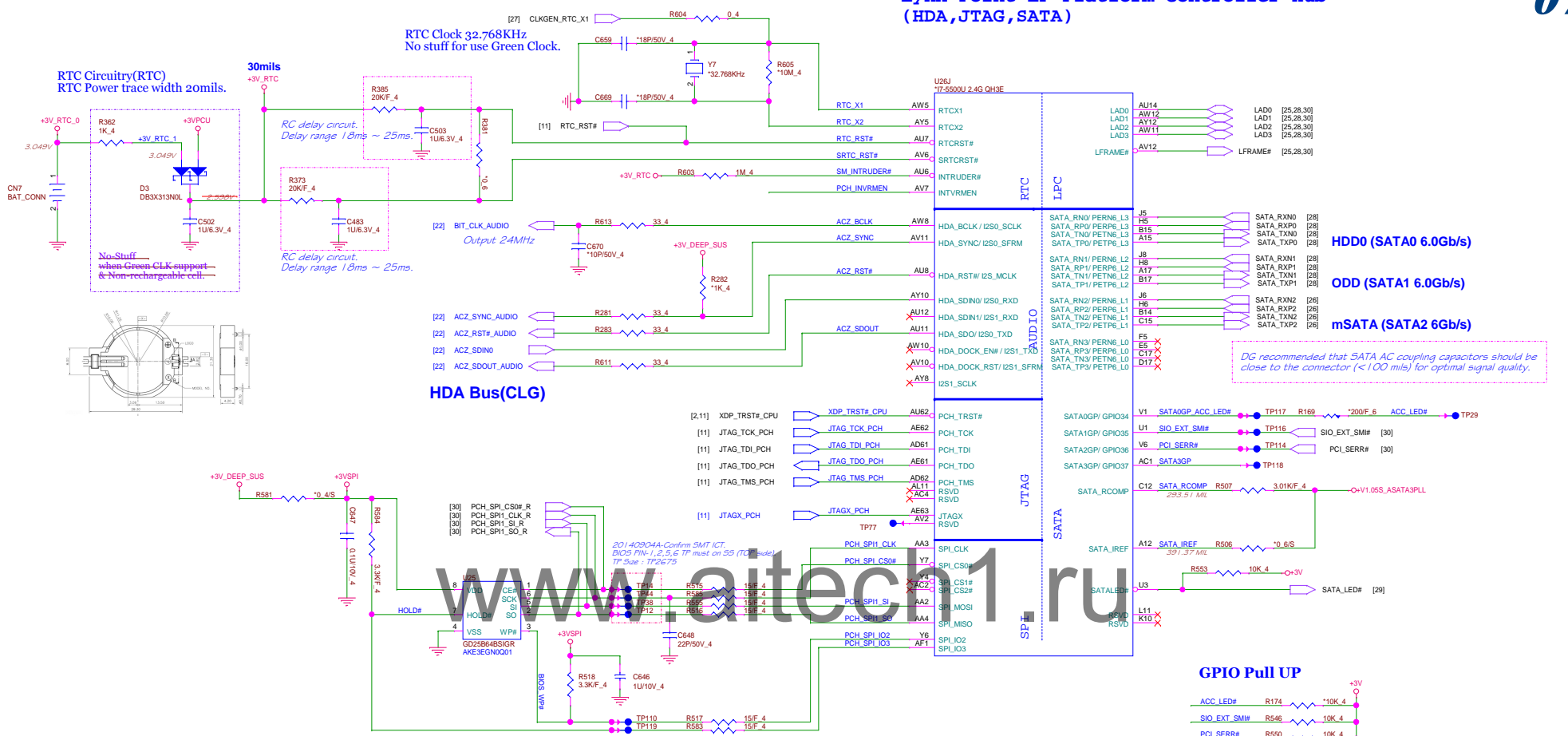
PCH Pull-high/low(CLG)



EDP HPD need pull down via 100KΩ, so combine with RTD2136 pin-1 DP HPD pull down resistor.
If only for eDP panel, EDP_HPDP must stuff one 100KΩ.

Reserve EDP_HPDP opposites circuit!

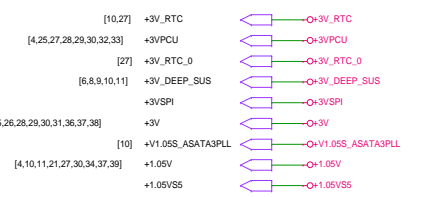
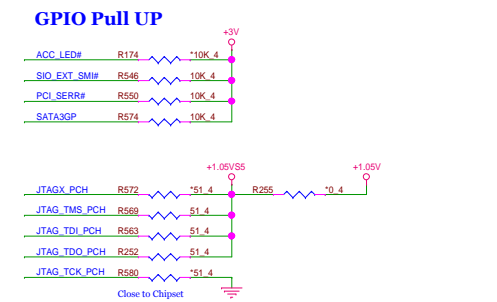
Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)



Vender	Size	P/N
AMIC	8MB	AKE3EFN0800 (A25LQ64M-F)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

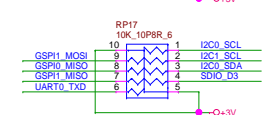
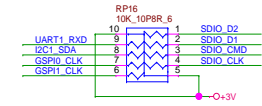
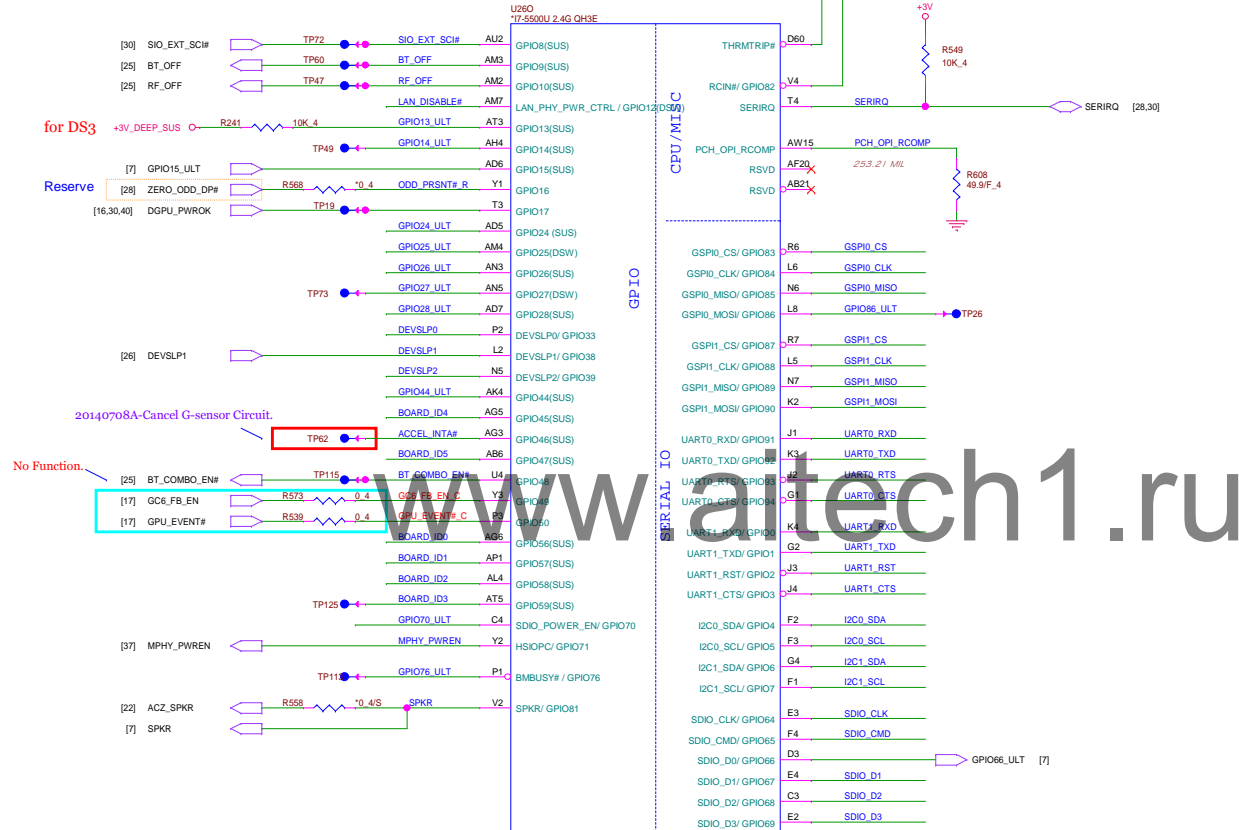
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0/GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden							
GSPI0_MOSI/GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNTO#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></tbody></table>	GNTO#	Boot Location	1	LPC	0	SPI(Default)	
GNTO#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up							

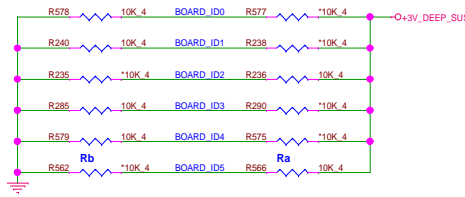
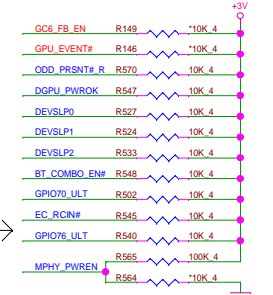
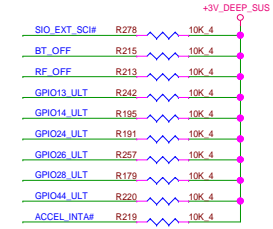


Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)

Haswell (GPIO)



GPIO Pull-up/Pull-down (CLG)

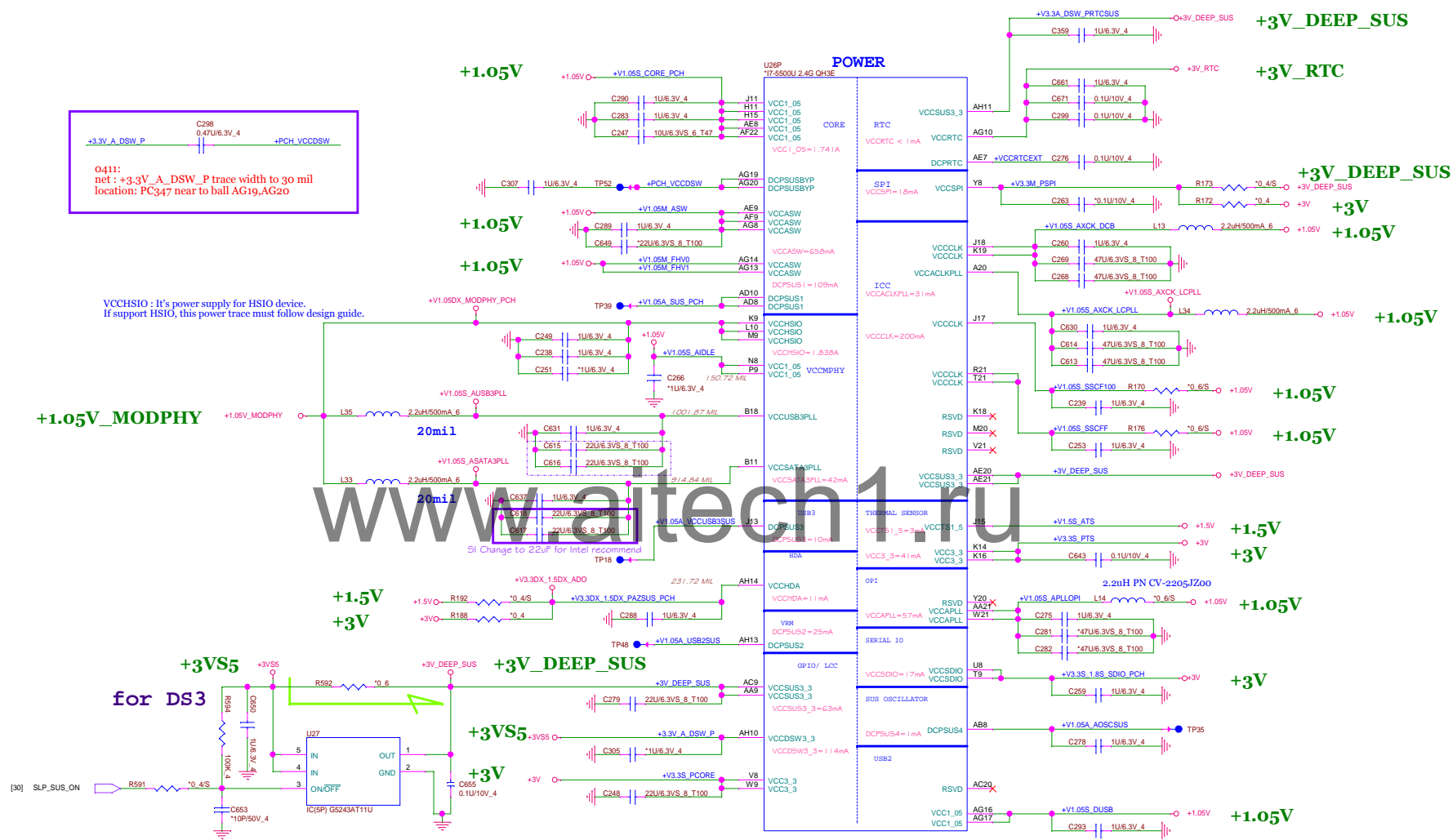














Model	BOARD_ID0 GPIO56 TWB : 0 JWV : 1	BOARD_ID1 GPIO57 No Define	BOARD_ID2 GPIO58 N16V : 0 N16S : 1	BOARD_ID3 GPIO59 No Define	BOARD_ID4 GPIO45 No Define	BOARD_ID5 GPIO47 UMA : 0 dGPU : 1
TWB + UMA	0	0	0	0	0	0
TWB + dGPU + N16S	0	0	1	0	0	1
TWB + dGPU + N16V	0	0	0	0	0	1
JWV + UMA	1	0	0	0	0	0
JWV + dGPU + N16S	1	0	1	0	0	1
JWV + dGPU + N16V	1	0	0	0	0	1

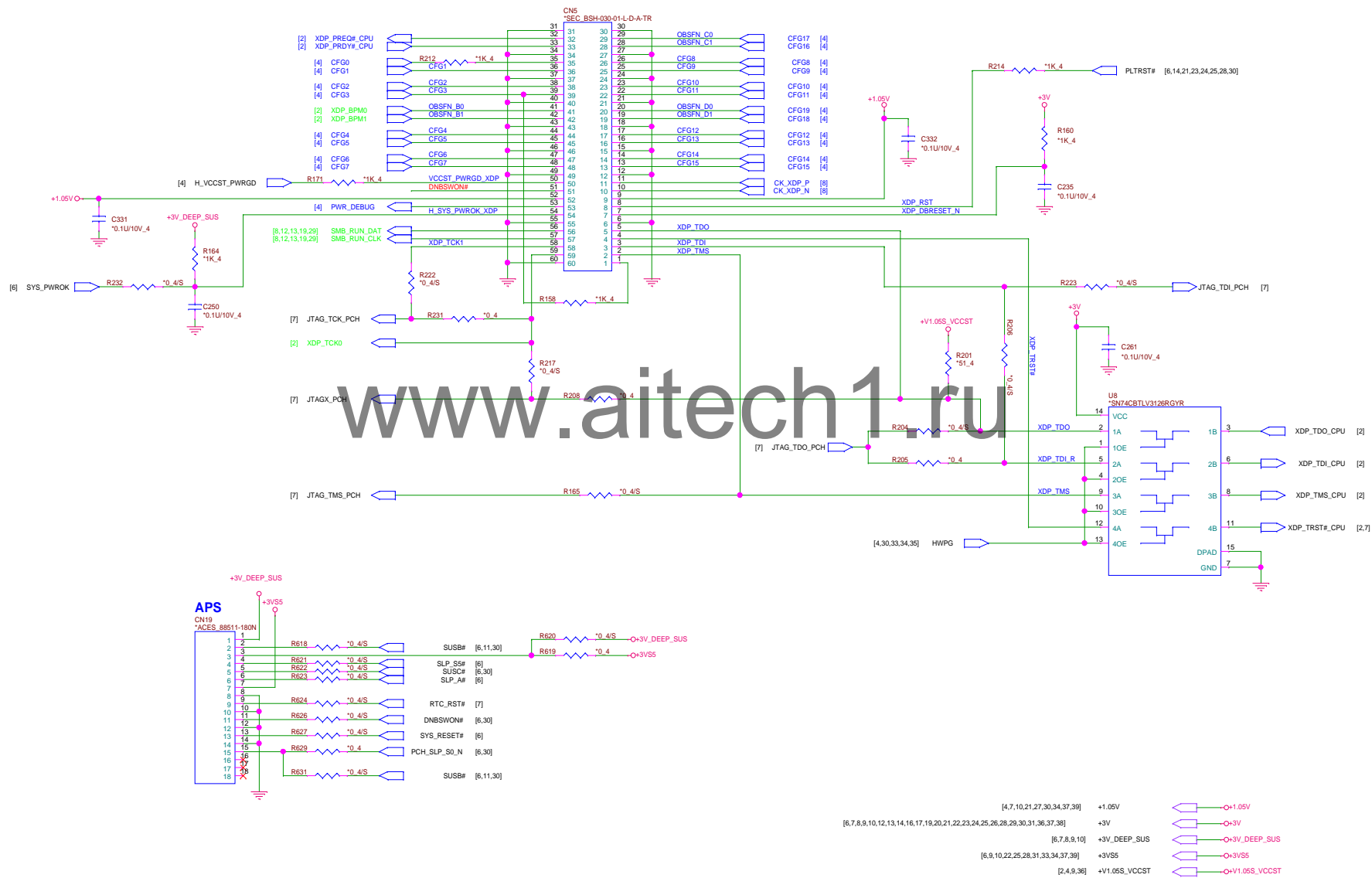
20141008A-BIOS request for SVID, N16S-GT need PU GPIO58 (BOARD_ID2).

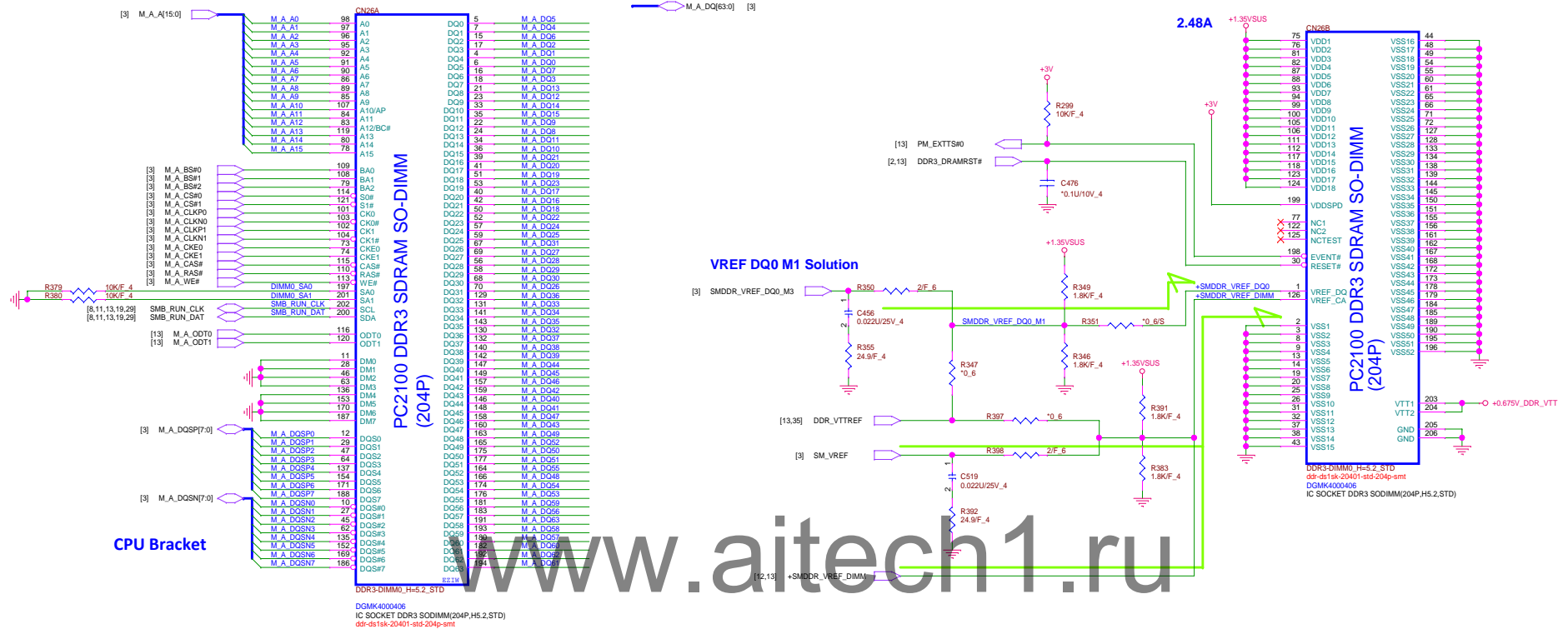
[2,4,11,36] +V1.05S_VCCST
[6,7,8,10,11] +3V_DEEP_SUS
[6,7,8,10,11,12,13,14,16,17,19,20,21,22,23,24,25,26,28,29,30,31,36,37,38] +3V
[6,10,11,22,25,28,31,33,34,37,38] +3V55

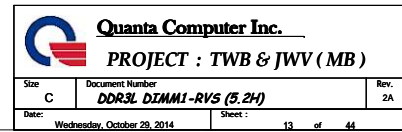
Lynx Point-LP Platform Controller Hub
(HDA,JTAG,SATA)(POWER)

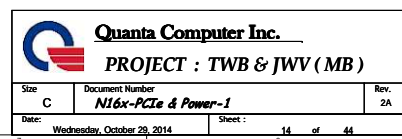


- | | | | |
|---------------------------------|----------------------|---|------------------------|
| [37] | +V1.05D_X_MODPHY_PCH |  | +O+V1.05D_X_MODPHY_PCH |
| [37] | +1.05V_MODPHY |  | +O+1.05V_MODPHY |
| [8] | +V1.05S_AXCK_LCPLL |  | +O+V1.05S_AXCK_LCPLL |
| | +V3.3D_X_1.5D_X_ADO |  | +O+V3.3D_X_1.5D_X_ADO |
| [8] | +V1.05S_AUSB3PLL |  | +O+V1.05S_AUSB3PLL |
| [7] | +V1.05S_ASATAS3PLL |  | +O+V1.05S_ASATAS3PLL |
| [6,7,8,9,11] | +3V_DEEP_SUS |  | +O+3V_DEEP_SUS |
| | [22,25,26,34] |  | +O+1.5V |
| 5,26,28,29,30,31,36,37,38] | +3V |  | +O+3V |
| 5,9,11,22,25,28,31,33,34,37,39] | +3VS5 |  | +O+3VS5 |
| | [7,27] |  | +O+3V_RTC |
| [4,7,11,21,27,30,34,37,39] | +1.05V |  | +O+1.05V |

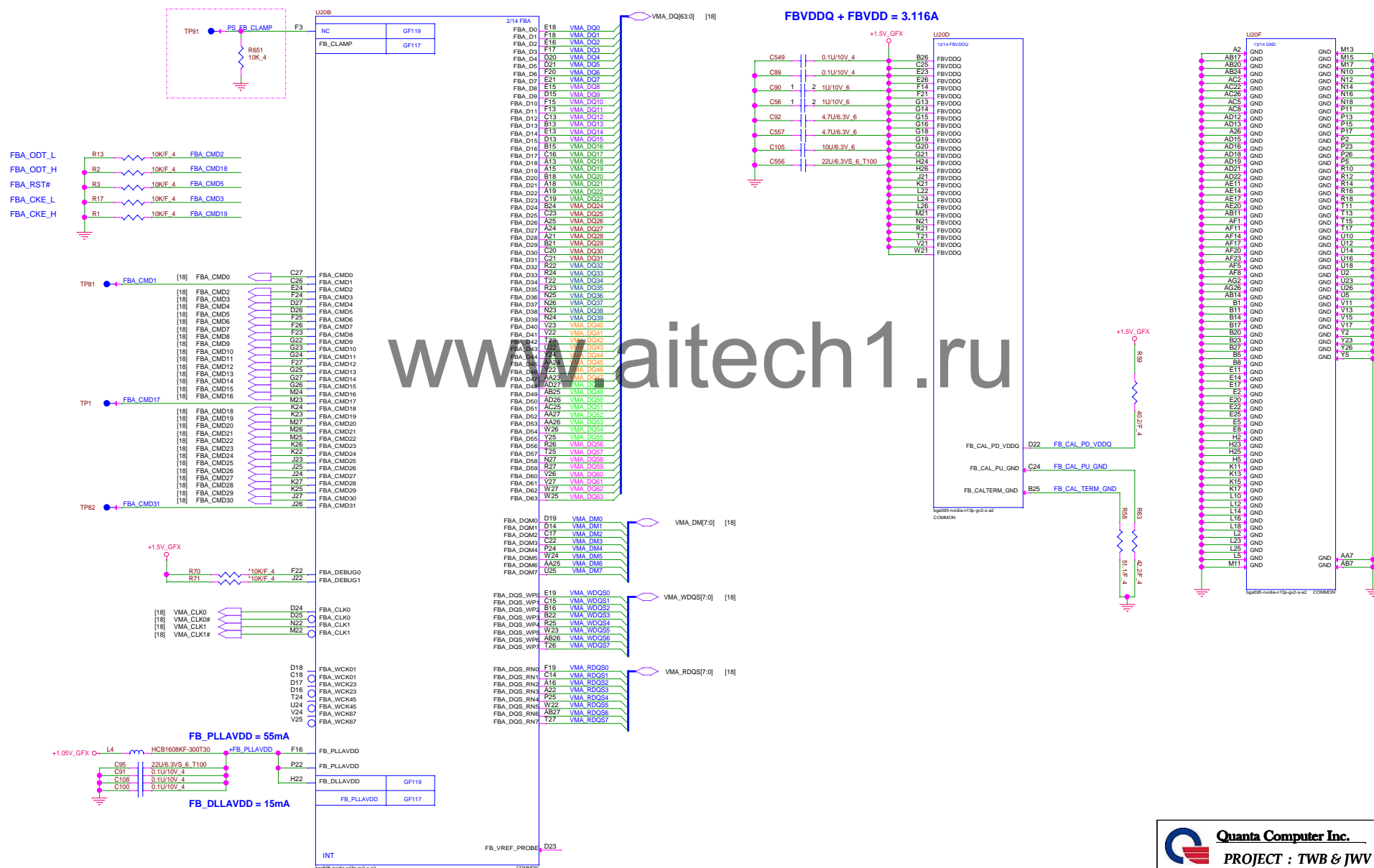


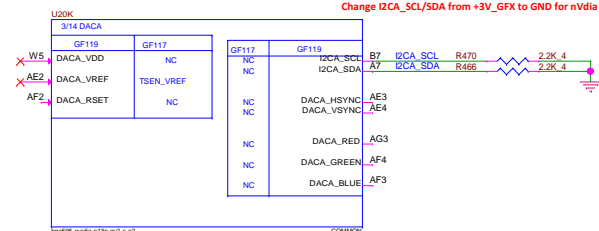
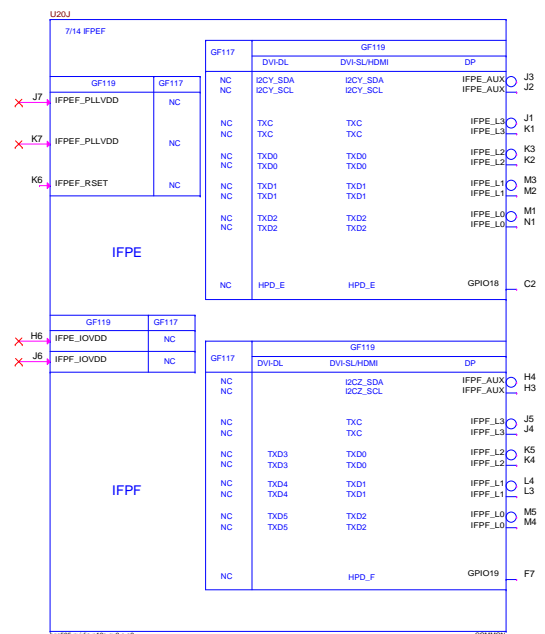




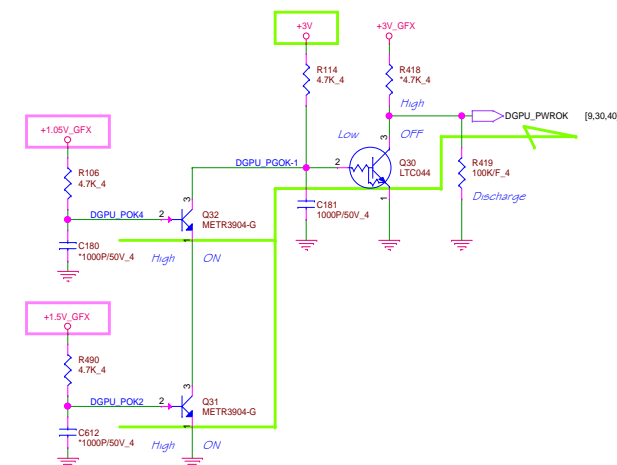
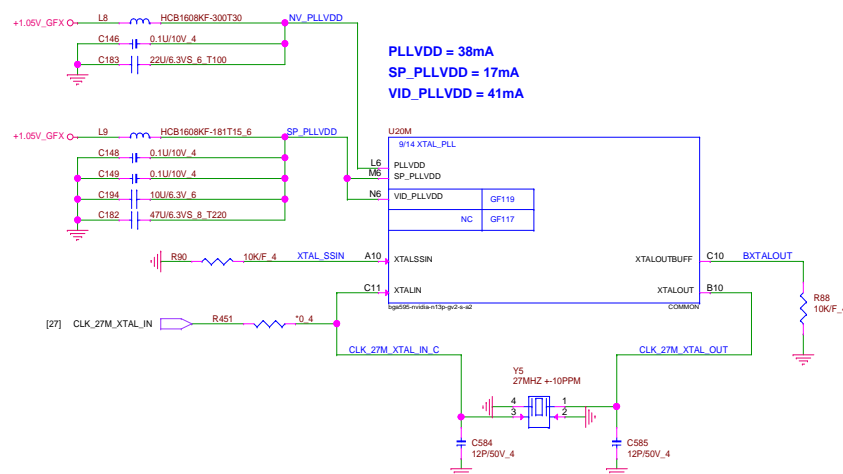
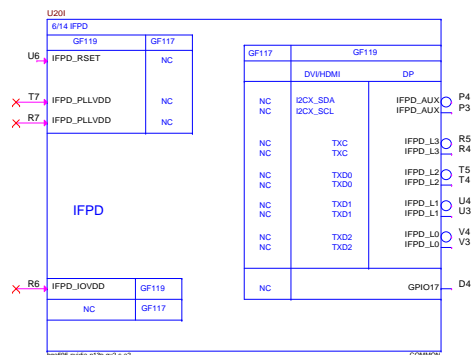
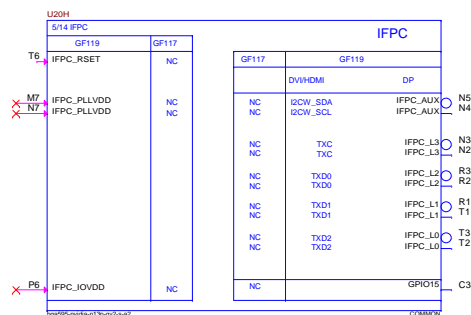


20140804A-NV recommend ball : F3 keep NC.
20140919A-NV recommend add 10K Ω PD on ball-F3 to avoid GPU entry GC6 I.O state when floating.
Some S3/S4 long run test fail is due to ball-F3 floating.





GPI/O	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY_VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



FUNCTION TABLE		Output $Y = A + B$
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H



* Only for 920M (N16V-GM)

Table 15-2. Resistance Mapping to Hex Values


ROM_SI (Memory strap setting)
BOM Default by 15K Ω PD for Samsung K4W4G1646D-BC1A for N16S-GT.
N16S-GT

Table 3. N16S-GM/-GT/-LP DDR3 Recommended Memories

N16V-GM DDR3 & DDR3L MEMORY RVL

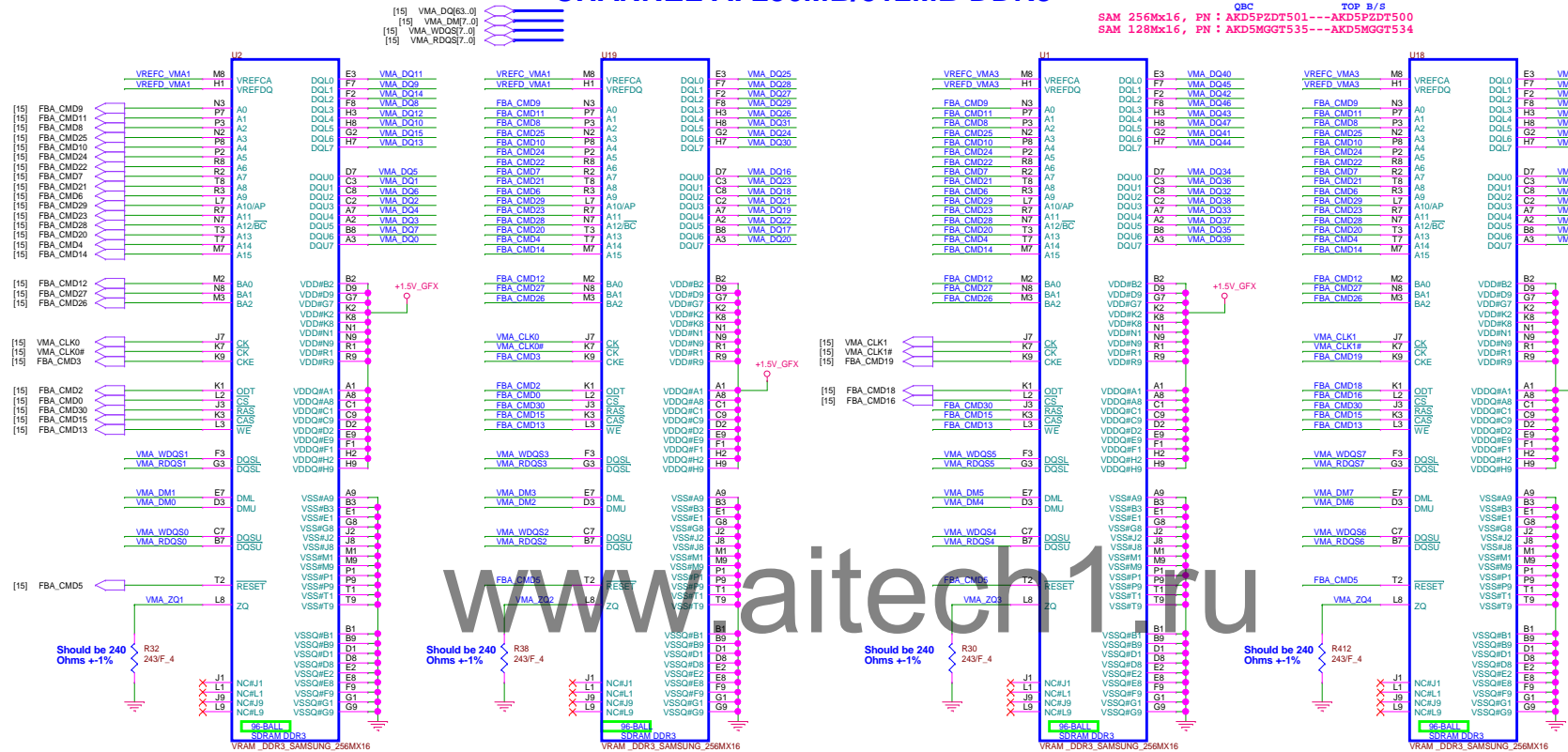
NVIDIA recommends the following DDR3 and DDR3L memories for use in conjunction with notebook designs using N16V-GM. **Note:** For H116V-GM, the maximum allowable memory case temperature is 85 °C.

Table 1. N16V-GM DDR3 Recommended Memories

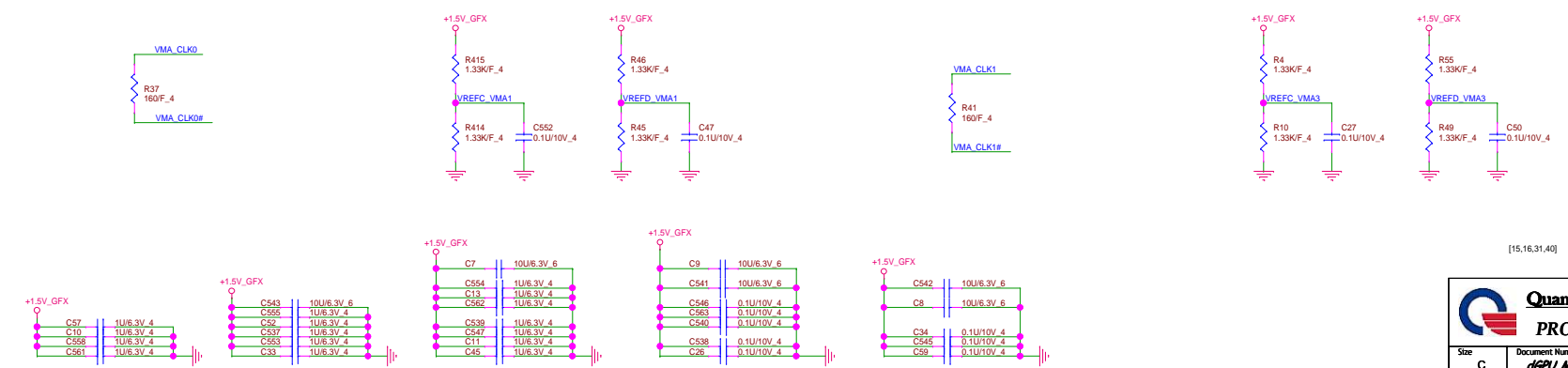
 Quanta Computer Inc. PROJECT : TWB & JWV (MB)		
Size C	Document Number NI6x-GPIO & Straps	
Date: Wednesday, October 28, 2014	Sheet : 17 of 44	

CHANNEL A: 256MB/512MB DDR3

HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02
QBC
SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534



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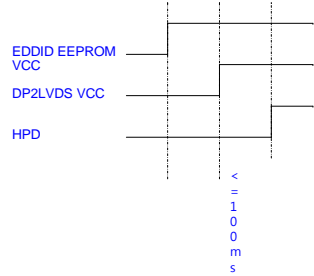


Follow TWE

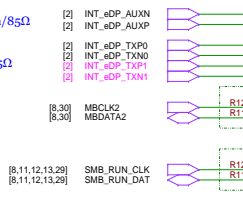
TWB/JWV default by LVDS circuit.

19

RTD2136S Power Up Sequence



AUX Channel : 6inch/85Ω
Main Link : 6inch/85Ω



5.1 Power On/Off Sequence

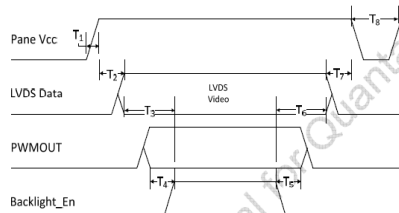


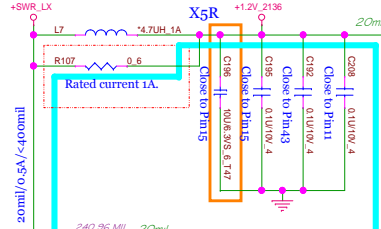
Figure 5-1 Panel On/Off Sequence

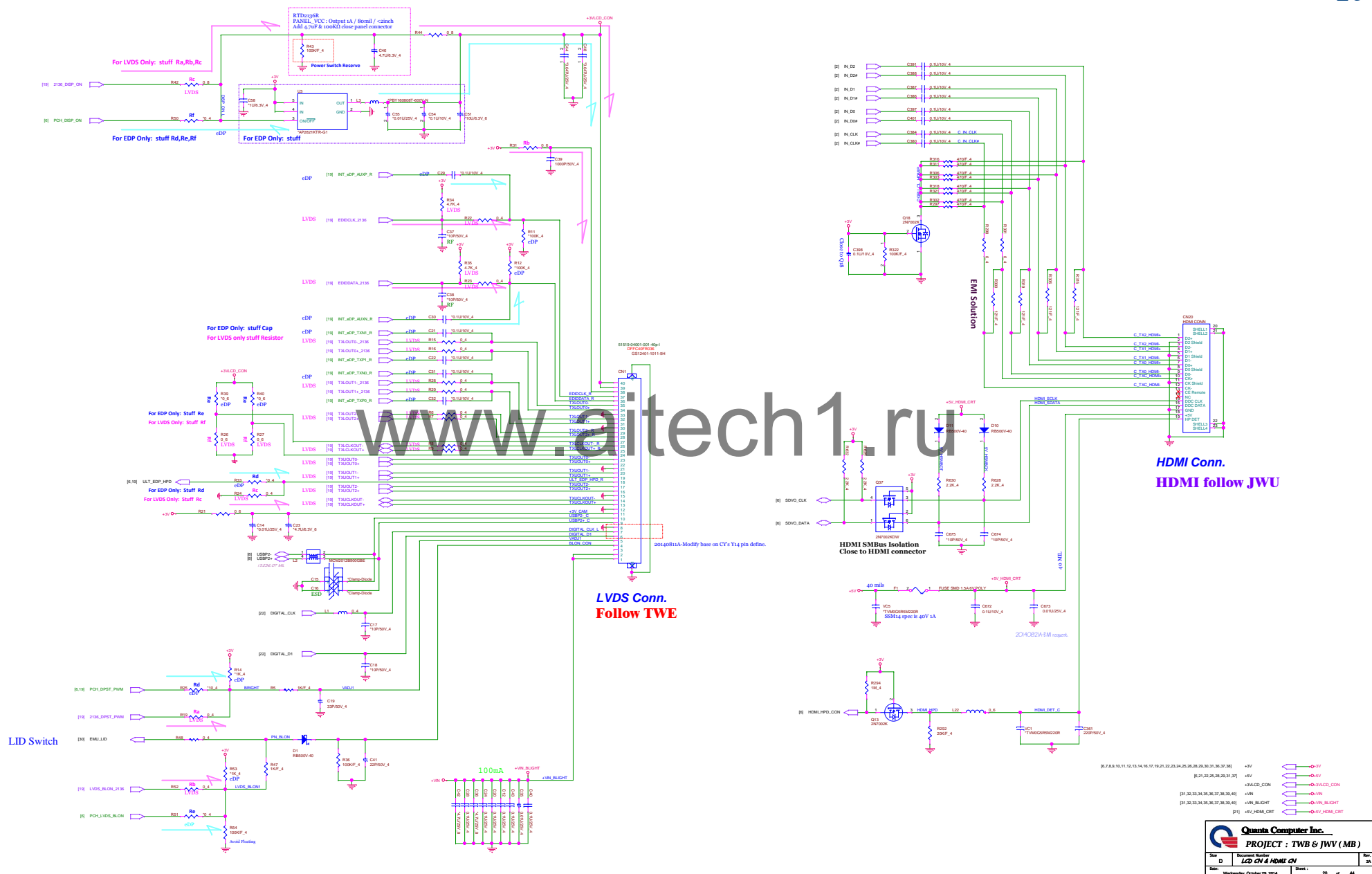
Table 5-1 Timing parameters of Power On/Off Sequence

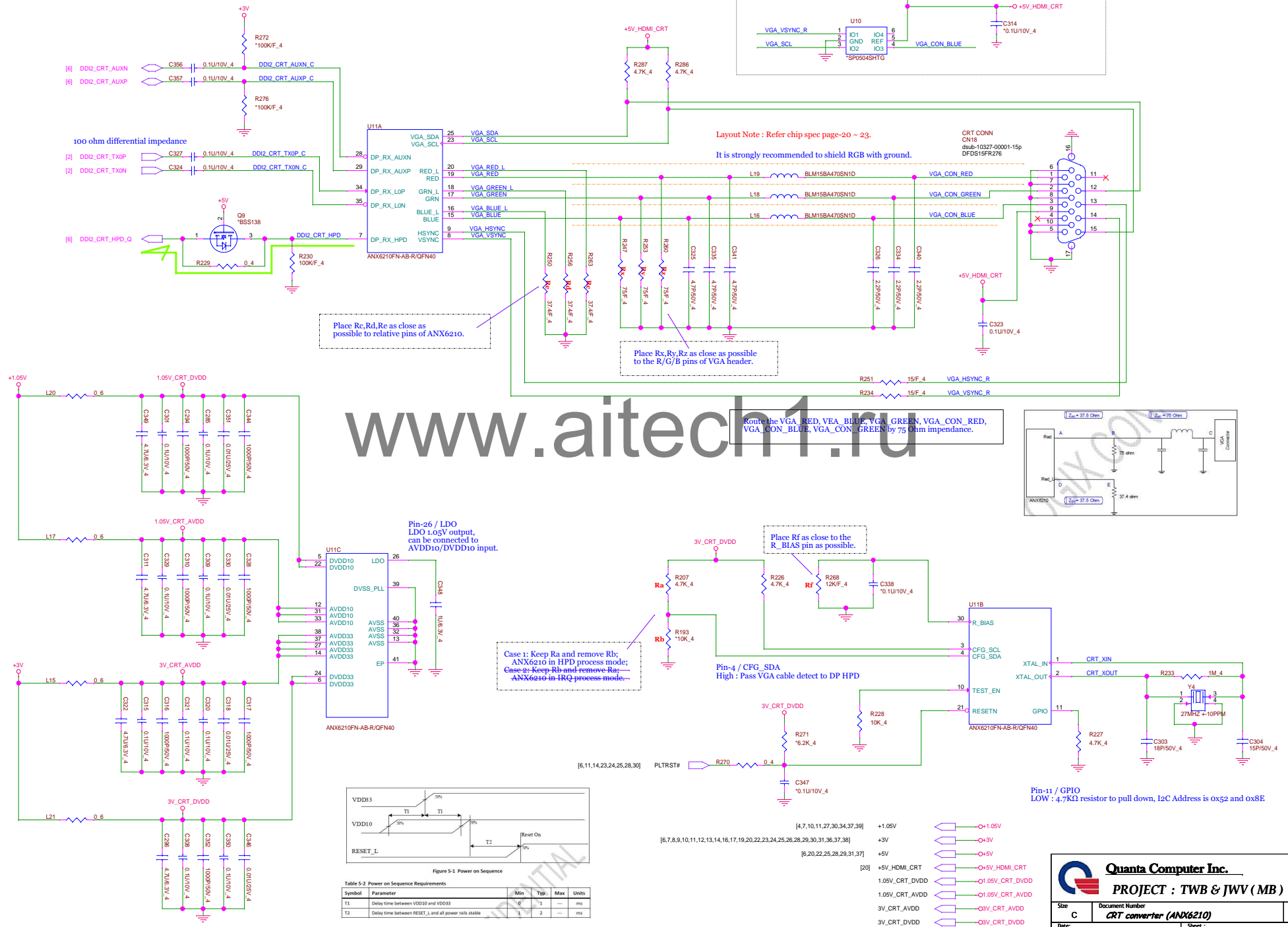
Time Para.	Description	Min.(ms)	Max.(ms)
T ₁	Rising time of Panel Vcc	0.5	10
T ₂	Delay from Panel Vcc output enable to LVDS output enable	0	50
T ₃	Delay from LVDS output enable to backlight output enable	200	—
T ₄	Delay from PWM output enable to backlight output enable	0	—
T ₅	Delay from backlight output disable to PWM output disable	0	—
T ₆	Delay from PWM output disable to LVDS output disable	200	—
T ₇	Delay from LVDS output disable to Panel Vcc output disable	0	50
T ₈	Delay between two power on/off sequence	500	—

SWR MODE	LDO MODE
Stuff inductance	Stuff Resister

L7: need use CV-4709MNOO for Vendor suggestion









9. Power Sequence

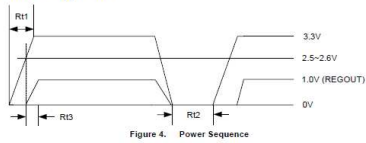
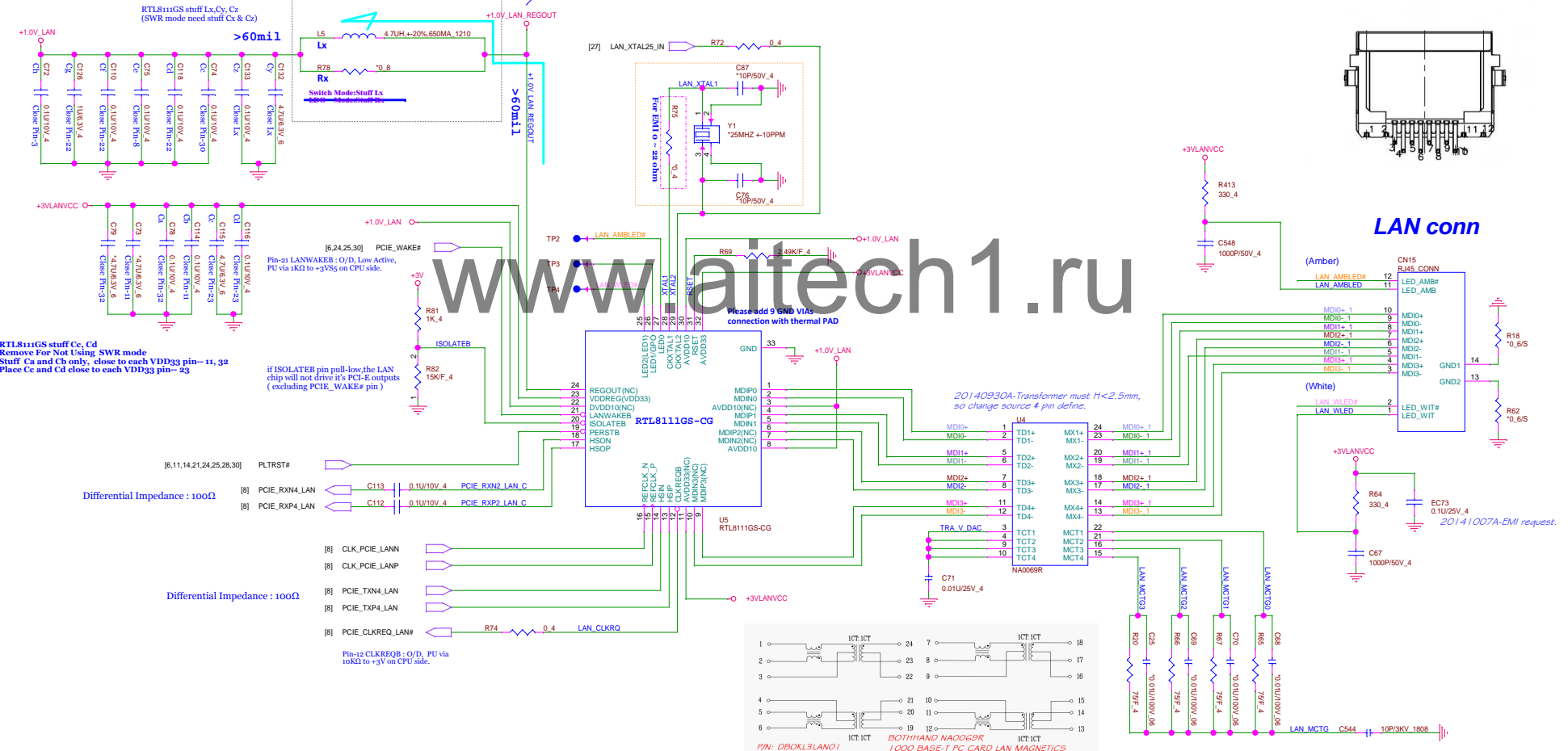


Table 16. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
R1	3.3V Rise Time	0.5	-	100	ms
R2	3.3V Off Time	50	-	-	ms
R3	1.0V (REGOUT) Settle Time	-	-	15	ms

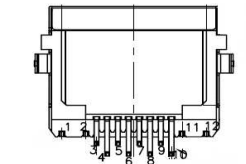
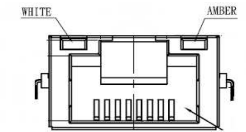
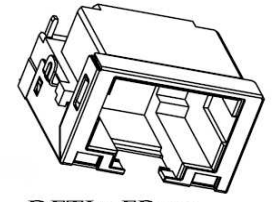
Note: See the following section for power sequence requirements.

Place Cc, Cd, Ce, Cf close to each VDD10 pin-- 3,8,22,30
Place Cg & Ch close to each VDD10 pin22

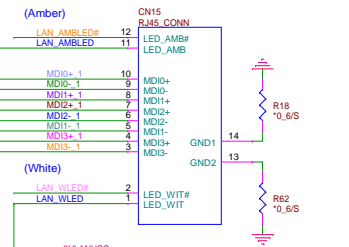


Pin	Name	Description	Cable Color
1	TX_D1+	Tranceive Data+	white/green
2	TX_D1-	Tranceive Data-	green
3	RX_D2+	Receive Data+	white/orange
4	BI_D3+	Bi-directional Data+	blue
5	BI_D3-	Bi-directional Data-	white/blue
6	RX_D2-	Receive Data-	orange
7	BI_D4+	Bi-directional Data+	white/brown
8	BI_D4-	Bi-directional Data-	brown

TX_D1+
TX_D1-
TX_D2+
TX_D3+
TX_D2-
TX_D4+
TX_D4-



LAN conn



Follow JW5

RTL8111GS: Switching Regulator
RTL8111G: LDO Regulator

Quanta Computer Inc. PROJECT : TWB & JWV (MB)		Rev. 2A
Size C	Document Number LAN-RTL8111GS-CG/RJ45	
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PIN-15	SP1	SD_D1	---	1/0	SD Data 1 (SD_D1)
PIN-16	SP2	SD_Do	MS_D1	1/0	SD Data 0 (SD_Do)
PIN-17	SP3	SD_CLK	MS_Do	1/0	SD Clock signal (SD_CLK)
PIN-19	SP4	SD_CMD	MS_D2	1/0	SD CMD signal (SD_CMD)
PIN-20	SP5	SD_D3	MS_D3	1/0	SD Data 3 (SD_D3)
PIN-21	SP6	SD_D2	MS_CLK	1/0	SD Data 2 (SD_D2)
PIN-29	SP7	SD_WP	MS_BS	1	SD Write Protect signal
PIN-30	SD_CD#	SD_CD#	---	1	SD Card Detection signal

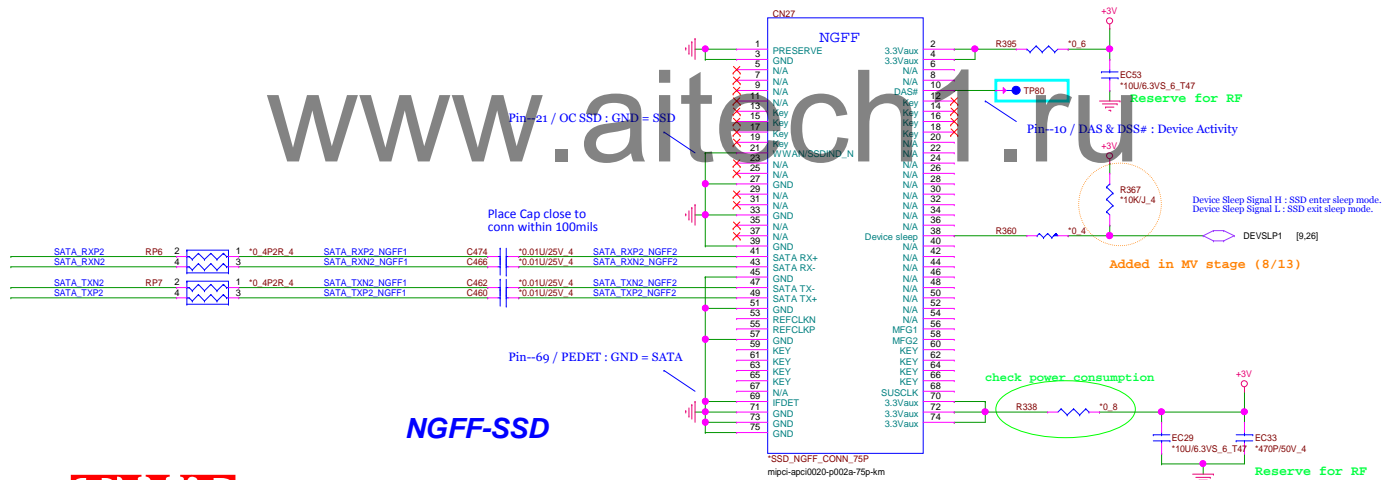
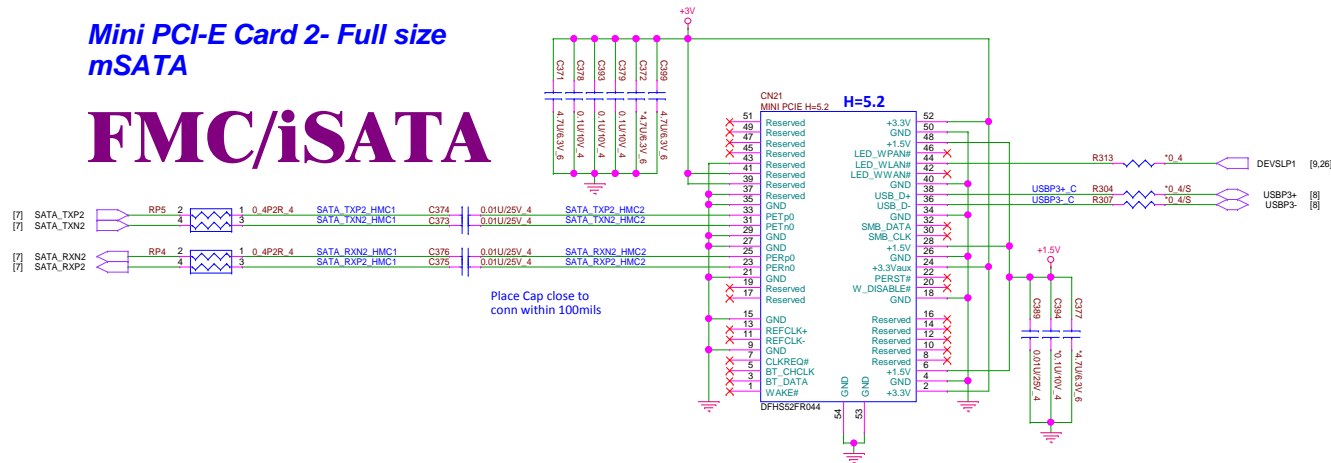


(Reserve) www.aitech1.ru



Mini PCI-E Card 2- Full size
mSATA

FMC/iSATA



Follow TWE
2280/2242

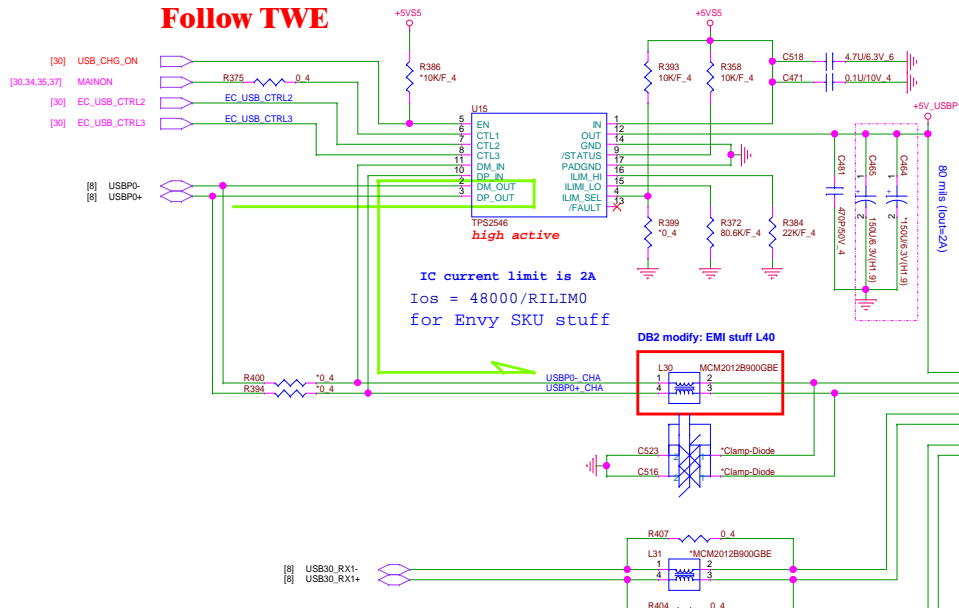
20140808-Change P/N & FP, must confirm pin define again.

mipci-apci0018-p002a-75p-kb

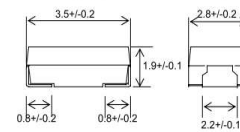
Input Voltage	Parameter	32GB	64GB	128GB	256GB	512GB
SATA 6Gb/s host interface						
5V ± 5%	Read [mW]	NA	2,600	2,700	2,800	TBD
	Write [mW]	NA	2,200	3,350	4,800	TBD
3.3V ± 5%	Read [mW]	2,200	2,450	2,650	2,650	NA
	Write [mW]	2,100	2,150	3,400	4,500	NA

Table 3-3: SanDisk SSD X110 Average Max Power Consumption

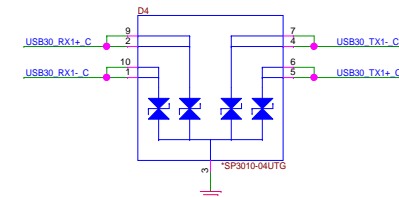
Follow TWE



Out view design (Dimensions : mm)

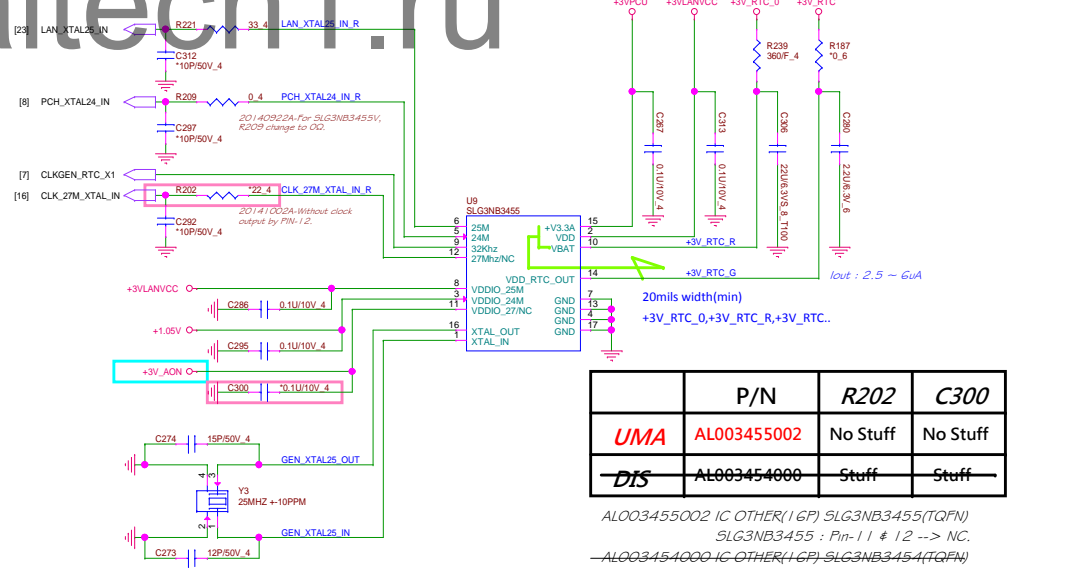


CH7151M8601
 CAP CHIP 150U
 6.3V(20%ESR35.3528.H1.9)



- [13,22,31,33,35,36,37,38,40] +5VSS
- [23,37] +3VLAVCC
- [4,7,10,11,21,30,34,37,38] +1.05V
- [4,7,25,28,29,30,32,33] +3VPCU
- [14,17,37] +3V_AON
- [7] +3V_RTC_0
- [7,10] +3V_RTC
- +5V_USBSP1
- +5V_USBSP0

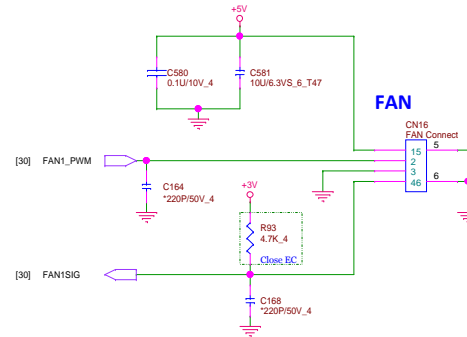
Green CLK Circuitry



	P/N	R202	C300
UMA	AL003455002	No Stuff	No Stuff
DIS	AL003454000	Stuff	Stuff

AL003455002 IC OTHER(1 GP) SLG3NB3455(TQFN)
 SLG3NB3455 : Pin-11 & 12 --> NC.
 AL003454000 IC OTHER(1 GP) SLG3NB3454(TQFN)

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



Bypass CAP close conn

3.3V 3.3V 3.3V 3.3V 5V 5V 5V 5V 12V 12V 12V 12V

GND1
GND2
GND3
GND
GND
GND
GND
GND
GND
GND
GND12
GND12
GND12
GND12

SATA TxP0_C
SATA TxN0_C
SATA RxN0_C
SATA RxP0_C

C683 0.01u/25V .4
C682 0.01u/25V .4
C681 0.01u/25V .4
C680 0.01u/25V .4

SATA TxP0 [7]
SATA TxN0 [7]
SATA RxN0 [7]
SATA RxP0 [7]

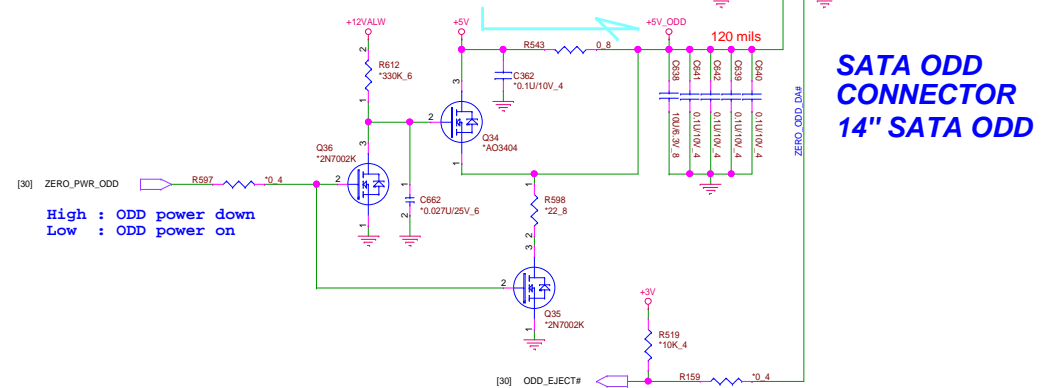
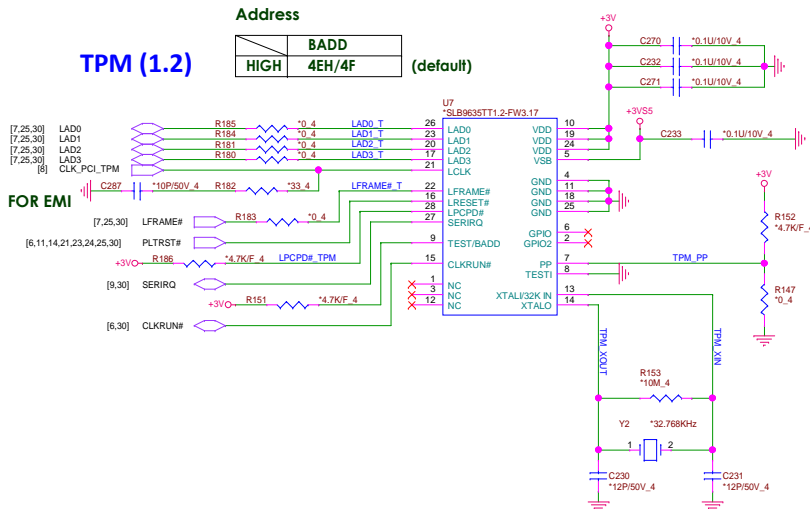
+3V : 2 A (4-Pin)
+5V : 2 A (4-Pin)

Gnd : (5 Pin)

The diagram shows a USB to UART conversion circuit. A USB cable is connected to a module labeled "FINGER PRINT CONN". The module has pins for USB4+, USB4-, USB4+, and USB4-. The circuit includes a 3.3V regulator (C365, 10.1U/10V, 4) and a 5V regulator (C366, 10.1U/10V, 4). The 3.3V line is connected to the USB4+ pin. The 5V line is connected to the USB4- pin. The module also has pins for TX, RX, and GND. The TX pin is connected to the RX pin. The RX pin is connected to the TX pin. The GND pin is connected to the GND pin. The module is labeled "20140821A-EMI request." and "88519-0001-4p4-smt DFFC06R112".

[illegible]

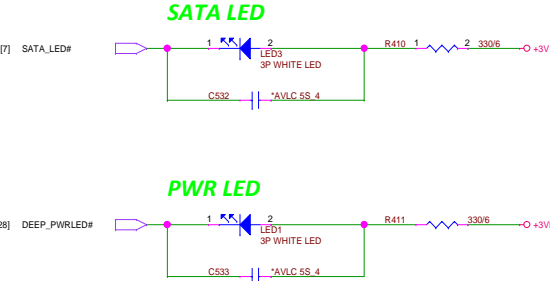
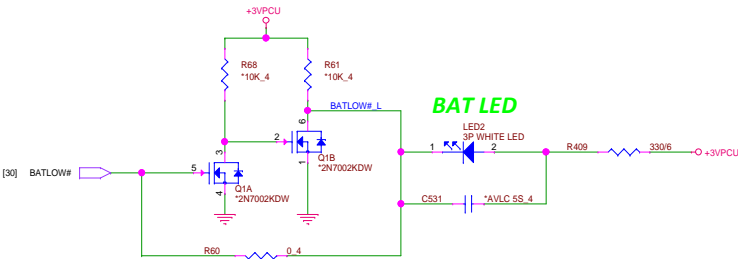
Address	
	BADD
HIGH	4EH/4F (default)



High : ODD power down
Low : ODD power on

**SATA ODD
CONNECTOR
14" SATA ODD**

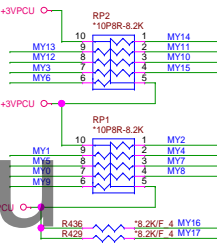
JWV remove G-sensor/Touch Screen function.



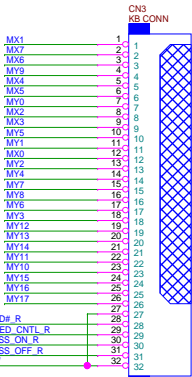
KEYBOARD Con.



KEYBOARD PULL-UP



0503 :
Change pin define and M/B keyboard connector follow R33

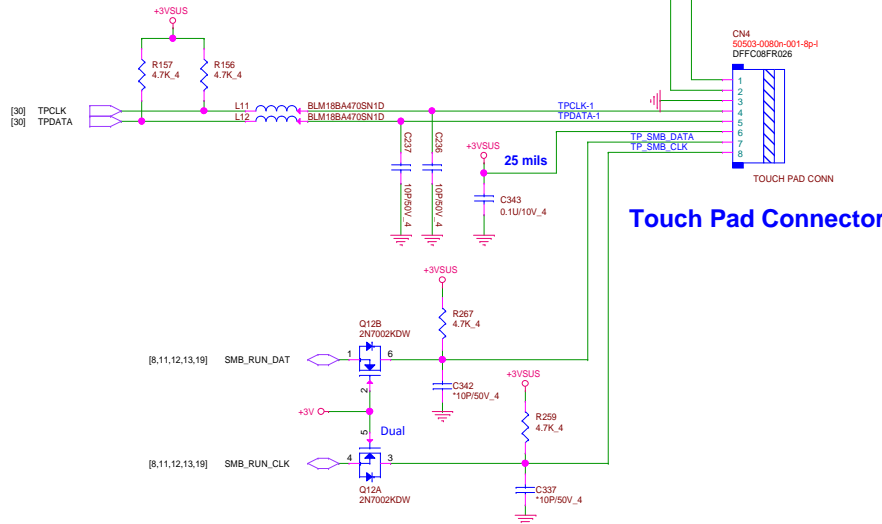


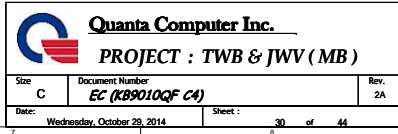
TWB 15" Left SW

JWV 14" Left SW

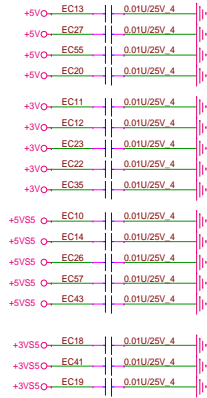
TWB 15" Right SW

JWV 14" Right SW

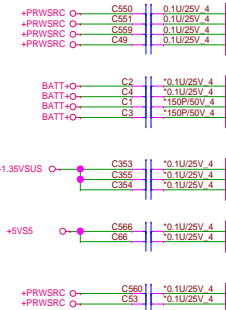
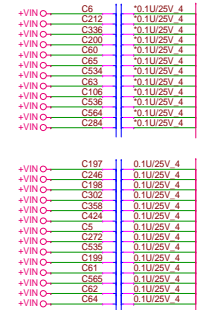
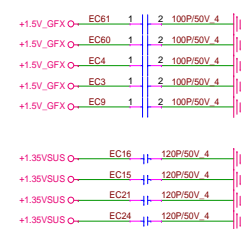




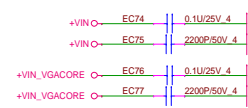
20140B29A-EMI request.



20140B26A-EMI request.



20140B26A-EMI request for PV.

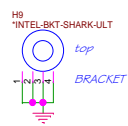


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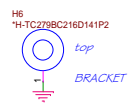
Hole

CPU BRACKET
P/N : FBUR6017010

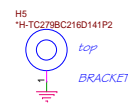
CPU Bracket

GPU BRACKET
P/N : FBR62021010

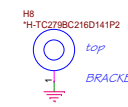
GPU Bracket



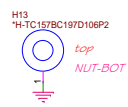
GPU Bracket



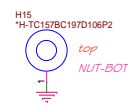
GPU Bracket

NGFF NUT
P/N : MBY01001010

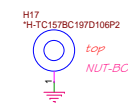
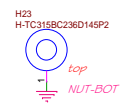
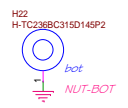
NGFF WLAN 2230



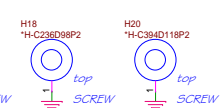
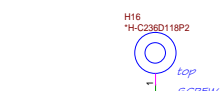
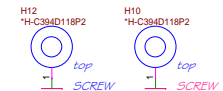
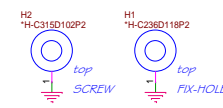
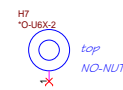
NGFF SSD 2240

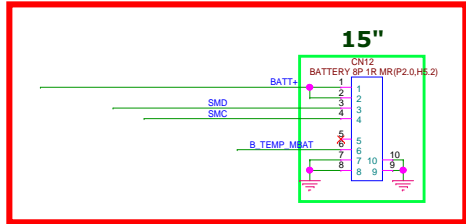


NGFF SSD 2280

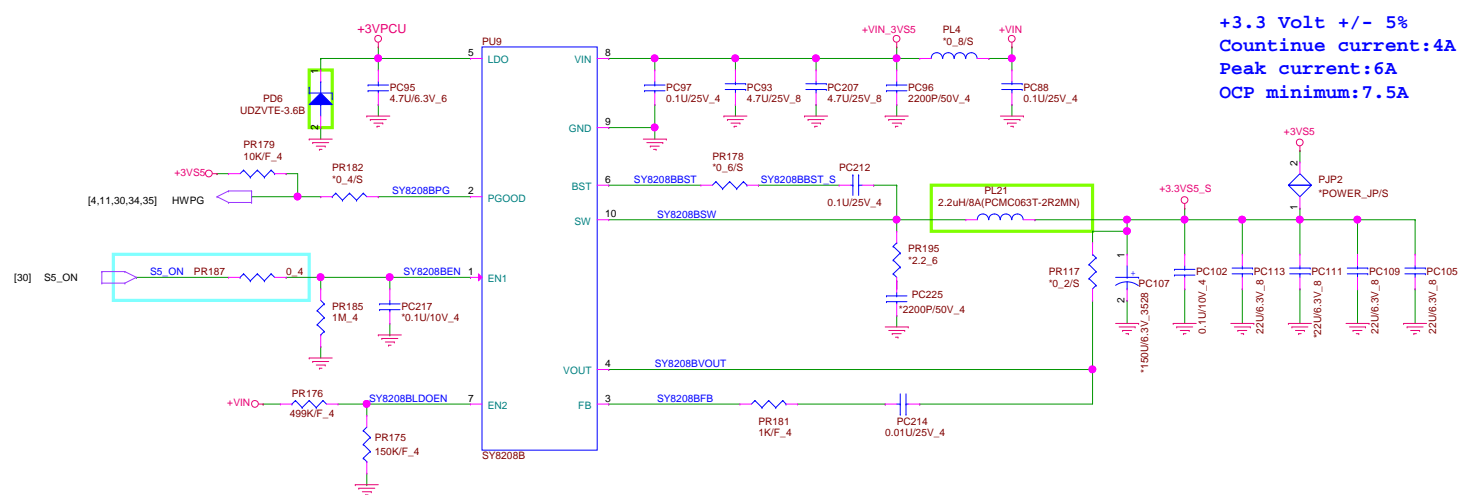
FAN NUT
P/N : MBFF4001010

Thermal Module





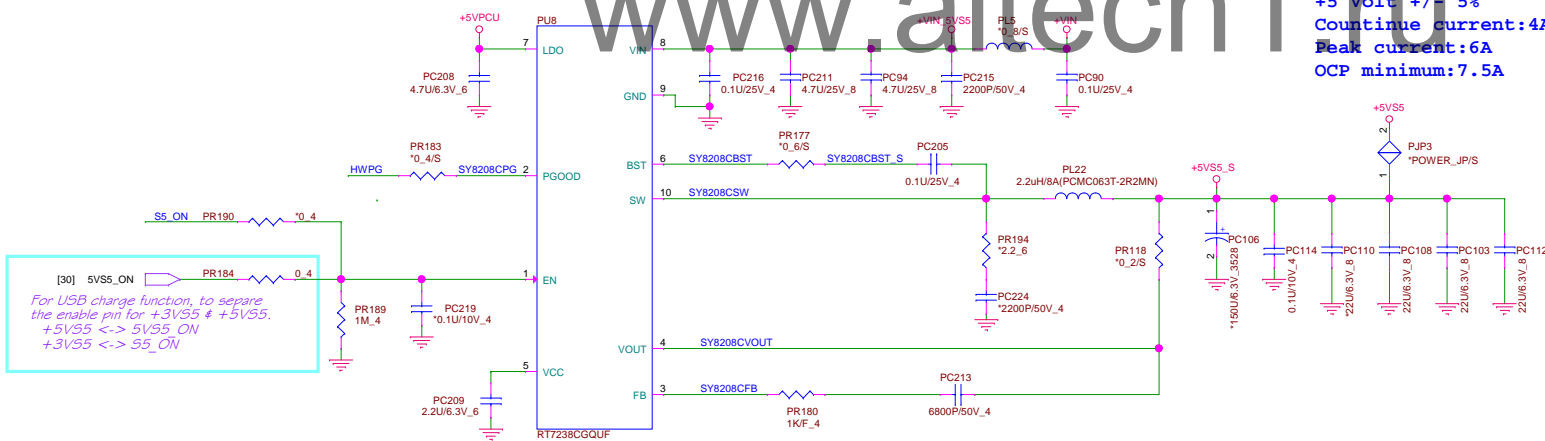
DC/DC +3VS5/+5VS5

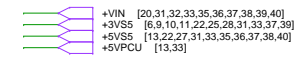


+3VS5 [6,9,10,11,22,25,28,31,34,37,39]
 +5VS5 [13,22,27,31,35,36,37,38,40]

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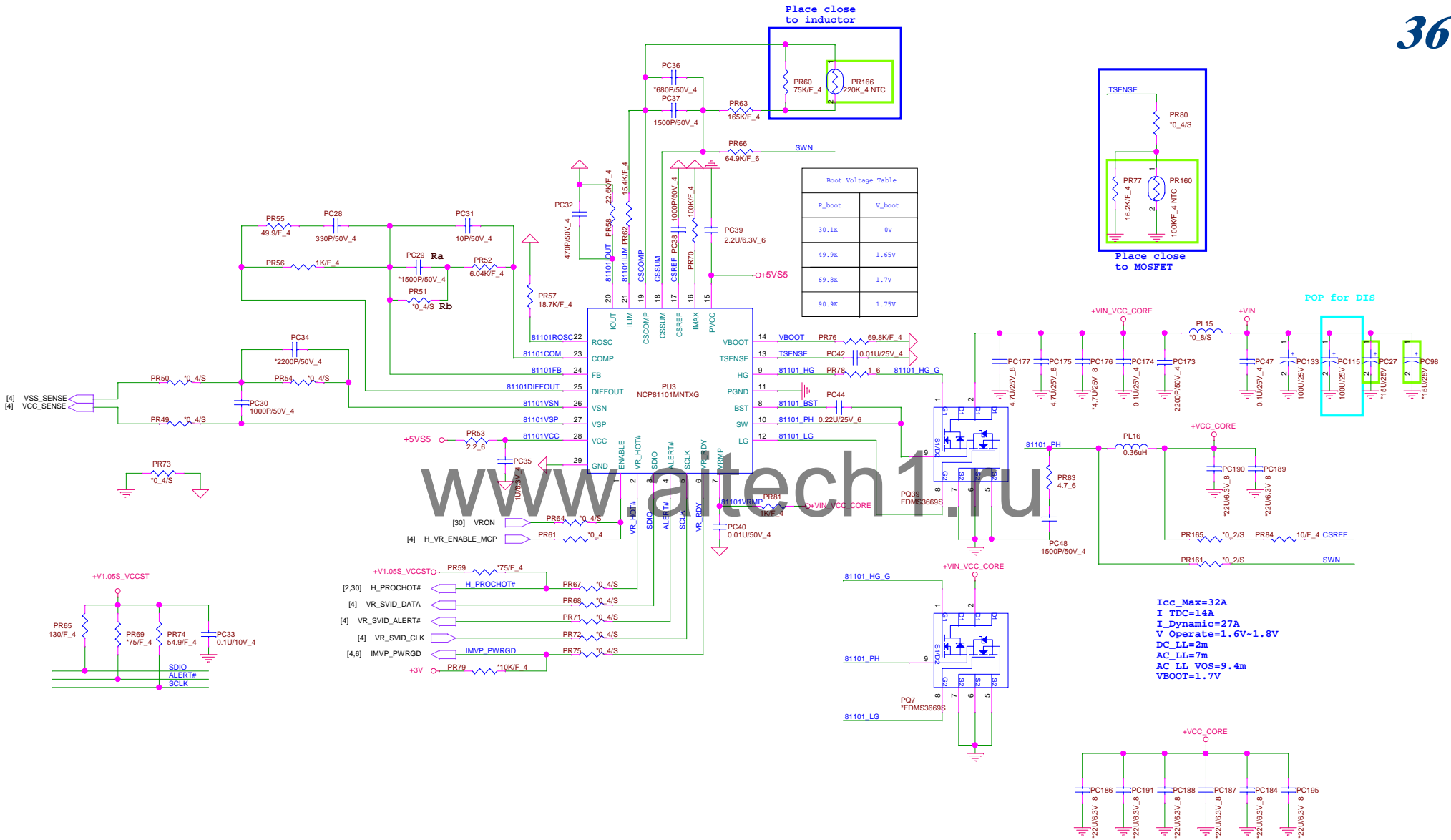
+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCp minimum:7.5A







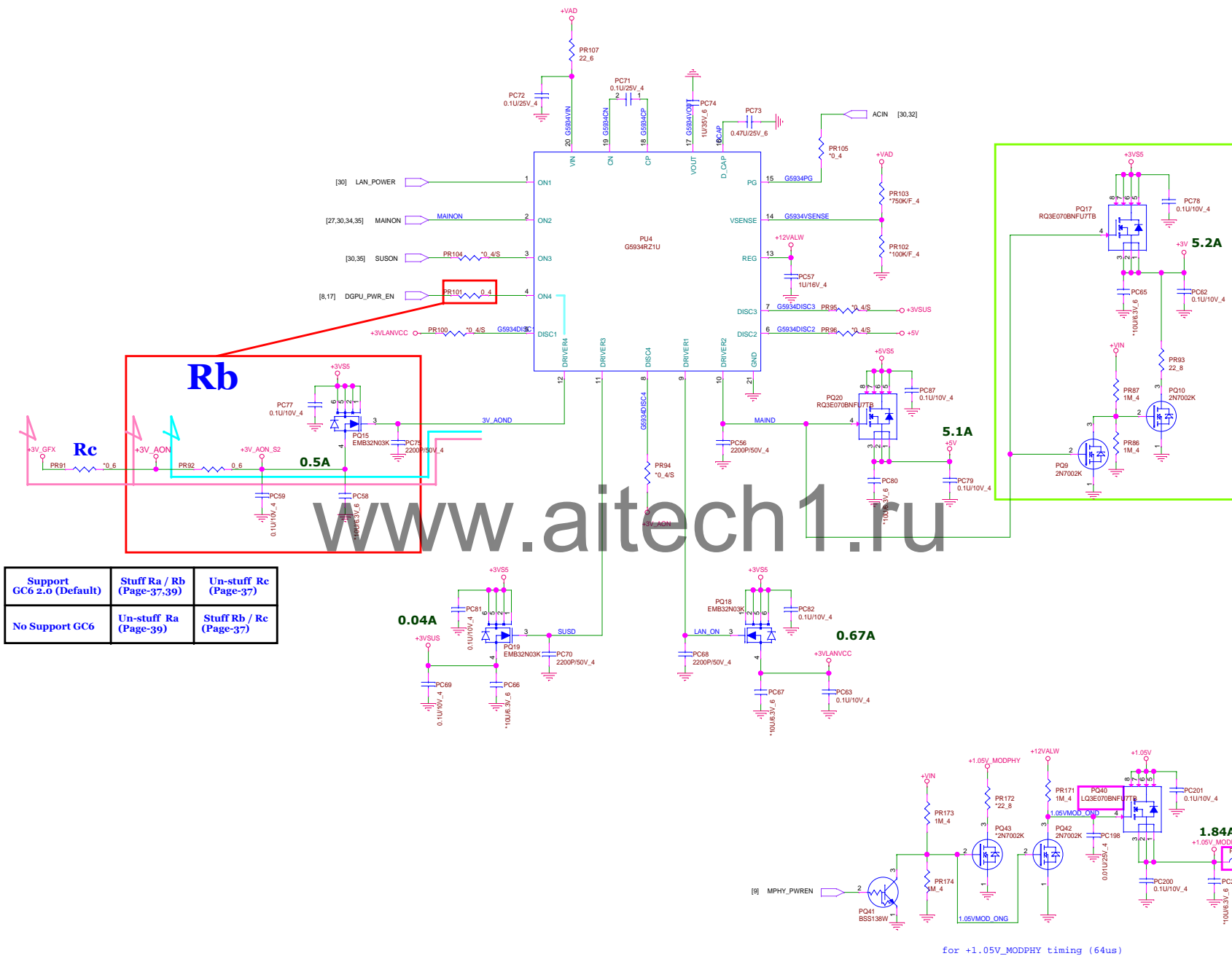
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



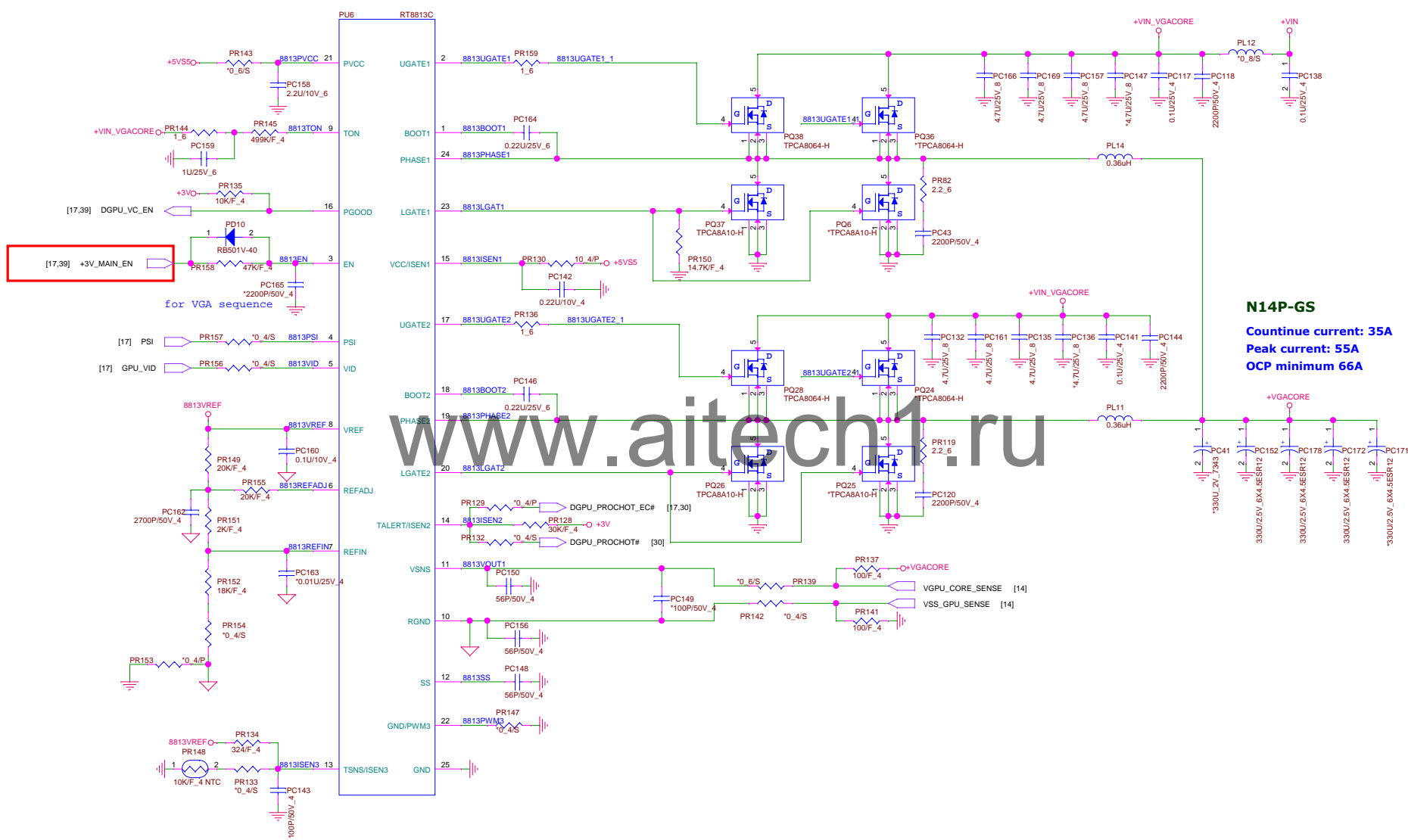
Quanta Computer Inc.

PROJECT : TWB & JWV (MB)

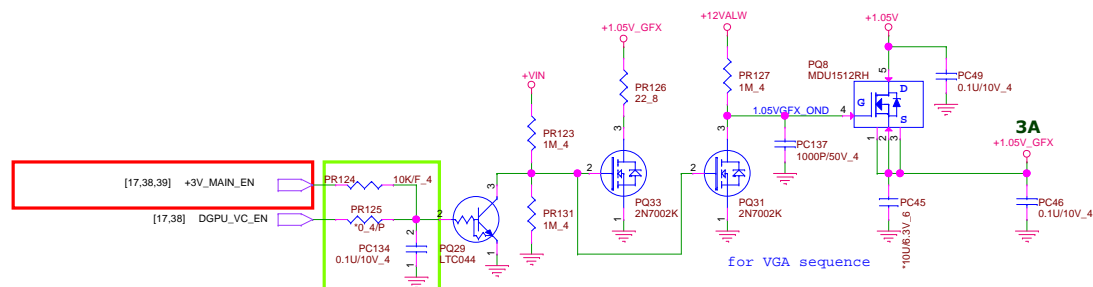
Size	Document Number	Rev.
Custom	CPU Core (NCP81101) ULT	2A
Date:	Wednesday, October 29, 2014	Sheet : 36 of 44

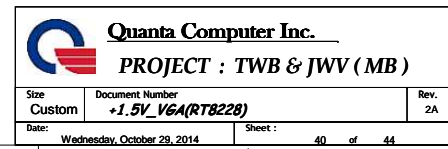


[6,7,8,9,10,11,12,13,14,16,17,19,20,21,22,23,24,25,26,28,29,30,31,36,38] +3V
 [20,31,32,33,34,35,36,38,39,40] +5V
 [6,8,10,11,22,25,26,31,33,34,39] +VIN
 [13,22,27,31,33,35,36,38,40] +3VS5
 [28,39] +12VALW
 [23,27] +3VLAVCC
 [12,13,35] +0.675V_DDR_VTT



N14P-GS
Countinue current: 35A
Peak current: 55A
OCP minimum 66A





USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT3	NC	N/A
PORT4	NC	N/A

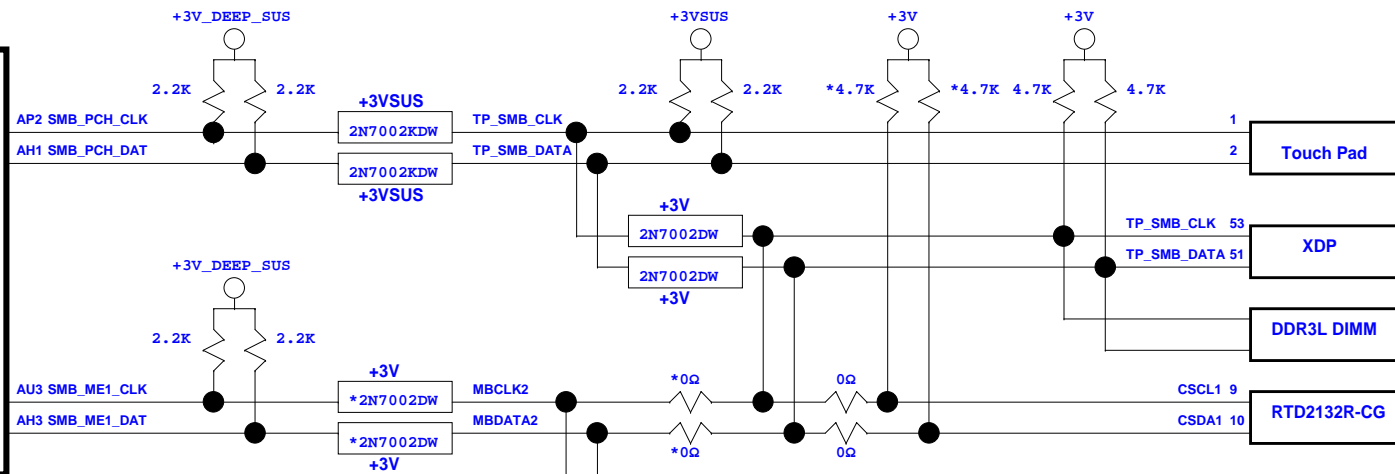
USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON#(from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON(from EC)

SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

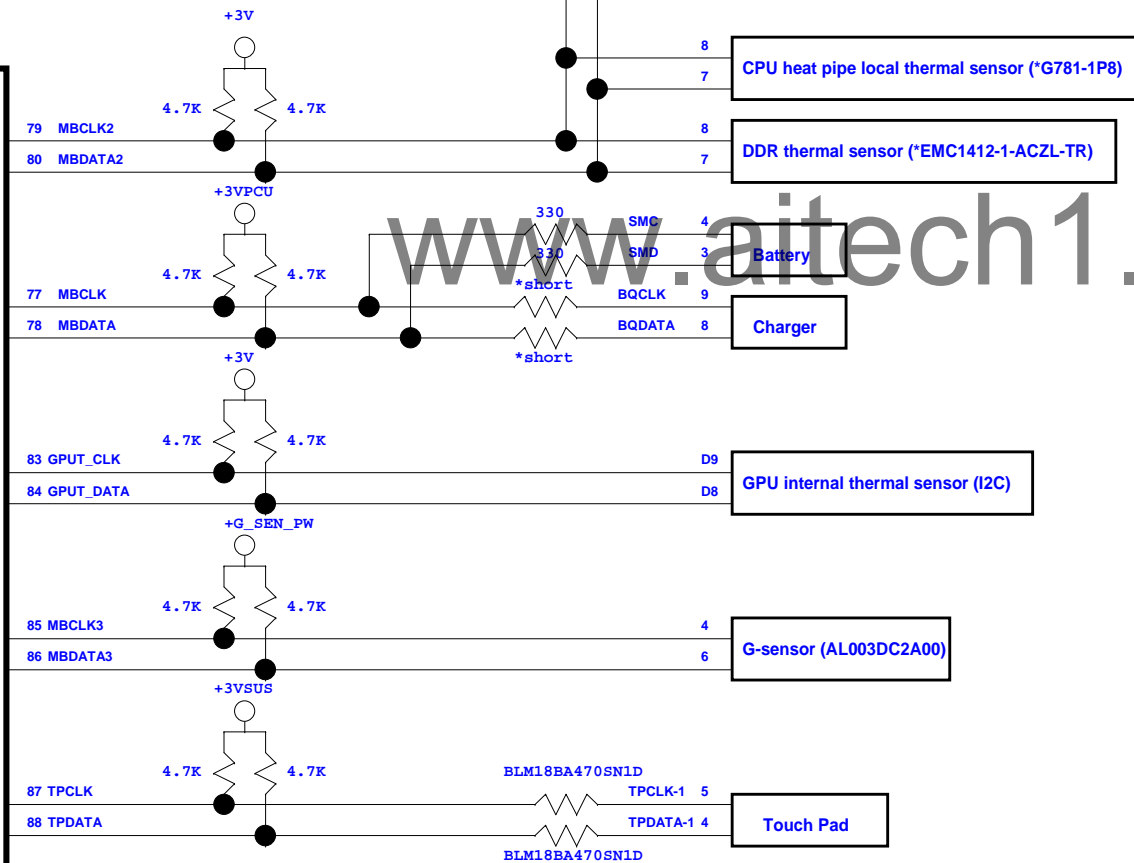
PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	

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